Description

The PLL QP RH is a Radiation Hardened by Design (RHBD) Phase Locked Loop available in ON Semiconductor ONC18 triple well process technology. ONC18 provides 180nm 1.8V CMOS with a number of variants to support analog, mixed-signal and dual gate oxide. RHBD addresses both Total Ionizing Dose (TID) and Single Event Latch-Up (SEL). The PLL is a general purpose clock source offering a wide range of user programmable output clock frequencies.

The PLL QP RH utilizes a single reference clock and produces two output clocks as shown in the functional block diagram below. The single output digital clock is a user programmable divided down version of the VCO oscillation frequency. The second output is a quad phase clock at the VCO oscillation frequency which is user programmable between 100MHz and 500MHz.

The reference clock divider and feedback divider ratio sets the VCO frequency. The output clock goes through a divider allowing the clock two be altered without adjusting the VCO oscillation frequency.

Features

- Large Output Clock Range (100Mhz-500Mhz)
- Quad Phase Output Clock
- Wide reference clock range (5Mhz-100Mhz)
- Differential VCO for good noise performance
- Additional programmable output clock

Applications

- Frequency Synthesize
- I/Q Modulated circuits requiring Quad Phase
- Precision Clock Multiplier
- System Reference Clock

Electrical and Physical Ratings

Power Supply	1.8V
Power Consumption	5mW
PLL Loop Bandwidth	200 KHz
Operating Temperature	-20°C to 85°C
Storage Temperature Range	-65°C to 150°C
Physical Block Area	0.15 mm^2

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Functional Block Diagram