Silicon Carbide (SiC) Module – 11 mohm SiC M3S MOSFET, 1200 V, TNPC Topology, F2 Package

Product Preview

NXH011T120M3F2PTHG

The NXH011T120M3F2PTHG is a power module containing an 11 mΩ / 1200 V SiC MOSFET TNPC and a thermistor with HPS DBC in an F2 package.

Features

- 11 mΩ / 1200 V M3S SiC MOSFET TNPC
- HPS DBC
- Thermistor
- Options with Pre−Applied Thermal Interface Material (TIM) and without Pre−Applied TIM
- Press−Fit Pins
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

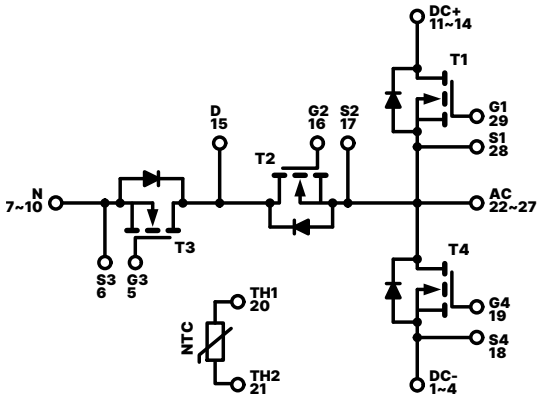
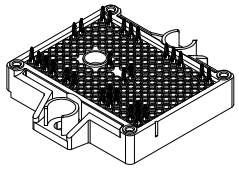


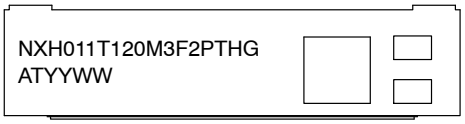
Figure 1. NXH011T120M3F2PTHG Schematic Diagram

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.



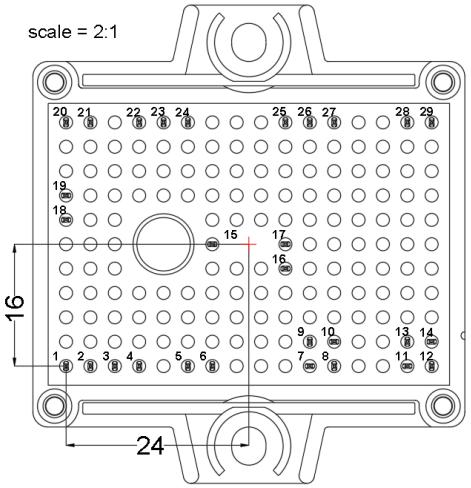
PIM29 56.7x42.5 (PRESS FIT)
CASE 180HR

MARKING DIAGRAM



NXH011T120M3F2PTHG = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	DC –	DC Negative Bus connection
2	DC –	DC Negative Bus connection
3	DC –	DC Negative Bus connection
4	DC –	DC Negative Bus connection
5	G3	T3 Gate
6	S3	T3 Source
7	N	DC Neutral Point
8	N	DC Neutral Point
9	N	DC Neutral Point
10	N	DC Neutral Point
11	DC+	DC Positive Bus connection
12	DC+	DC Positive Bus connection
13	DC+	DC Positive Bus connection
14	DC+	DC Positive Bus connection
15	D	Common point drain
16	G2	T2 Gate
17	S2	T2 Source
18	S4	T4 Source
19	G4	T4 Gate
20	TH1	Thermistor Connection 1
21	TH2	Thermistor Connection 2
22	AC	AC Phase Output
23	AC	AC Phase Output
24	AC	AC Phase Output
25	AC	AC Phase Output
26	AC	AC Phase Output
27	AC	AC Phase Output
28	S1	T1 Source
29	G1	T1 Gate

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain−Source Voltage	V_{DSS}	1200	V
Gate−Source Voltage	V_{GS}	+22/−10	V
Continuous Drain Current @ T_c = 80°C (T_J = 175°C)	I_D	91	A
Pulsed Drain Current (T_J = 175°C) (Note 2)	I_{Dpulse}	273	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	272	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
TIM Layer Thickness	T_{TIM}	160 ± 20	μm
INSULATION PROPERTIES			
Isolation test voltage, t = 1 sec, 60 Hz	V_{is}	4800	V_{RMS}
Creepage distance		12.7	mm
CTI		600	
Substrate Ceramic Material		HPS	
Substrate Ceramic Material Thickness		0.38	mm
Substrate Warpage (Note 2)	W	Max 0.18	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Height difference between horizontal plane and substrate copper bottom.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V	I_{DSS}	–	–	300	μA
Drain−Source On Resistance	V_{GS} = 18 V, I_D = 70 A, T_J = 25°C	$R_{DS(ON)}$	–	11.9	16	mΩ
	V_{GS} = 18 V, I_D = 70 A, T_J = 125°C		–	21.5	–	
	V_{GS} = 18 V, I_D = 70 A, T_J = 150°C		–	24.1	–	
	V_{GS} = 18 V, I_D = 70 A, T_J = 175°C		–	28.1	–	
Gate−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 40 mA	$V_{GS(TH)}$	1.8	2.8	4.4	V
Gate Leakage Current	V_{GS} = −10 V / 20 V, V_{DS} = 0 V	I_{GSS}	−600	–	600	nA
Input Capacitance	V_{DS} = 800 V, V_{GS} = 0 V, f = 100 kHz	C_{ISS}	–	6331	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	29	–	
Output Capacitance		C_{OSS}	–	354	–	

ELECTRICAL CHARACTERISTICS (continued)
T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Total Gate Charge	V_{DS} = 800 V, V_{GS} = −5/20 V, I_D = 200 A	$Q_{G(TOTAL)}$	–	306	–	nC
Gate−Source Charge		Q_{GS}	–	31	–	nC
Gate−Drain Charge		Q_{GD}	–	78	–	nC
SiC MOSFET CHARACTERISTICS − Halfbridge Commutation Path						
Turn−on Delay Time	T_J = 25°C V_{DS}= 400 V, I_D = 70 A V_{GS} = −3 V / 18 V, R_G = 2.7 Ω	$t_{d(on)}$	–	40.1	–	ns
Rise Time		t_r	–	14.5	–	
Turn−off Delay Time		$t_{d(off)}$	–	111.3	–	
Fall Time		t_f	–	10.4	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.33	–	mJ
Turn−off Switching Loss per Pulse		E_{OFF}	–	0.13	–	
Turn−on Delay Time	T_J = 150°C V_{DS} = 400 V, I_D = 70 A V_{GS} = −3 V / 18 V, R_G = 2.7 Ω	$t_{d(on)}$	–	38	–	ns
Rise Time		t_r	–	12.81	–	
Turn−off Delay Time		$t_{d(off)}$	–	124	–	
Fall Time		t_f	–	12.2	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.38	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	0.17	–	
Diode Forward Voltage	I_D = 70 A, T_J = 25°C, V_{GS} = −3 V	V_{SD}	–	5.18	6.5	V
	I_D = 70 A, T_J = 125°C, V_{GS} = −3 V		–	4.78	–	
	I_D = 70 A, T_J = 150°C		–	4.72	–	
Thermal Resistance − Chip−to−Case	T1, T2, T3, T4	R_{thJC}	–	0.349	–	°C/W
Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil +2%, A = 2.8 W/mK	R_{thJH}	–	0.548	–	°C/W
SiC MOSFET CHARACTERISTICS − Neutral Point Commutation Path						
Turn−on Delay Time	T_J = 25°C V_{DS}= 400 V, I_D = 70 A V_{GS} = −5 V / 18 V, R_G = 2.7 Ω	$t_{d(on)}$	–	40.8	–	ns
Rise Time		t_r	–	13.8	–	
Turn−off Delay Time		$t_{d(off)}$	–	112.6	–	
Fall Time		t_f	–	8.7	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.34	–	mJ
Turn−off Switching Loss per Pulse		E_{OFF}	–	0.18	–	
Turn−on Delay Time	T_J = 150°C V_{DS} = 400 V, I_D = 70 A V_{GS} = −3 V / 18 V, R_G = 2.7 Ω	$t_{d(on)}$	–	38.4	–	ns
Rise Time		t_r	–	12.0	–	
Turn−off Delay Time		$t_{d(off)}$	–	137	–	
Fall Time		t_f	–	8.9	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.38	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	0.23	–	
THERMISTOR CHARACTERISTICS						
Nominal Resistance	TNTC = 25°C	R_{25}	–	5	–	kΩ
	TNTC = 100°C	R_{100}	–	493	–	Ω
	TNTC = 150°C	R_{150}	–	159.5	–	Ω
Deviation of R100	TNTC = 100°C	ΔR/R	−5	–	5	%

ELECTRICAL CHARACTERISTICS (continued)
T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
THERMISTOR CHARACTERISTICS						
Power Dissipation − Recommended Limit	0.15 mA. Non−Self−heating Effect	P_D	−	0.1	−	mW
Power Dissipation − Absolute Maximum	5 mA	P_D	−	34.2	−	mW
Power Dissipation Constant			−	1.4	−	mW/K
B−value	B(25/50), tolerance ±2%		−	3375	−	K
B−value	B(25/100), tolerance ±2%		−	3436	−	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH011T120M3F2PTHG	NXH011T120M3F2PTHG	F2−TNPC: Case 180HR Press−fit Pins with pre−applied thermal interface material (TIM) (Pb-Free / Halide Free)	20 Units / Blister Tray

TYPICAL CHARACTERISTICS

M1/M2 SIC MOSFET CHARACTERISTIC

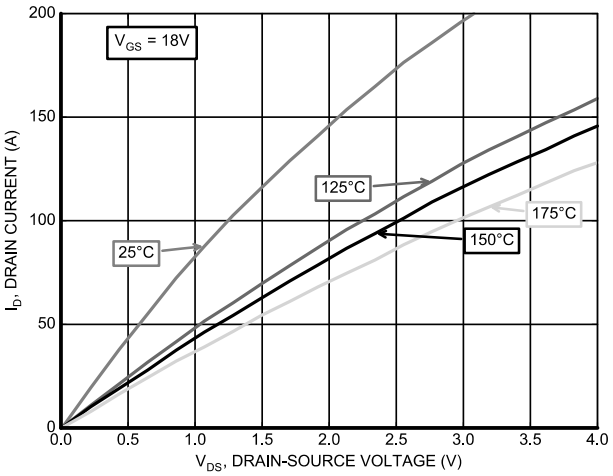


Figure 2. MOSFET Typical Output Characteristic

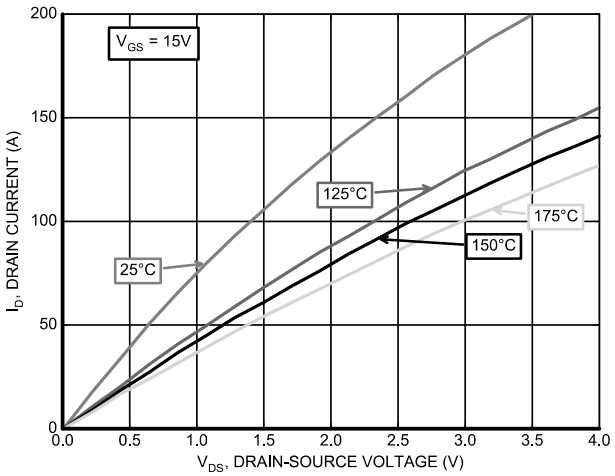


Figure 3. MOSFET Typical Output Characteristic

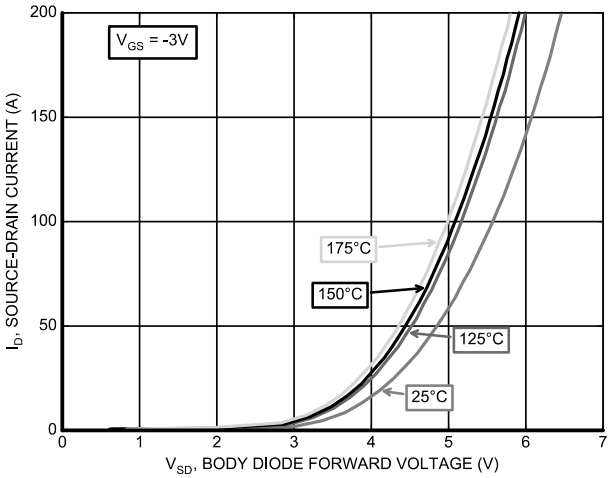


Figure 4. I_D vs. V_{SD}

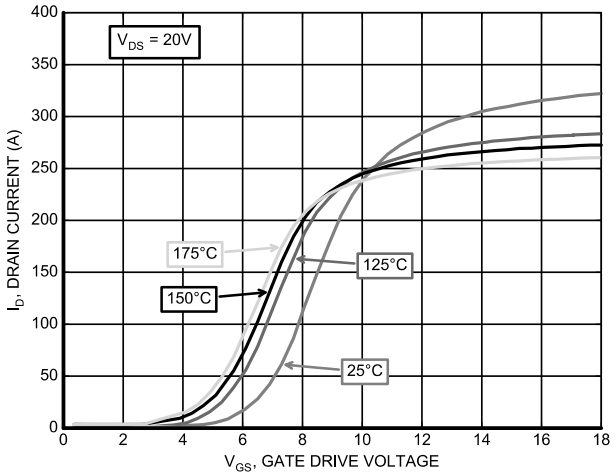


Figure 5. I_D vs. V_{GS}

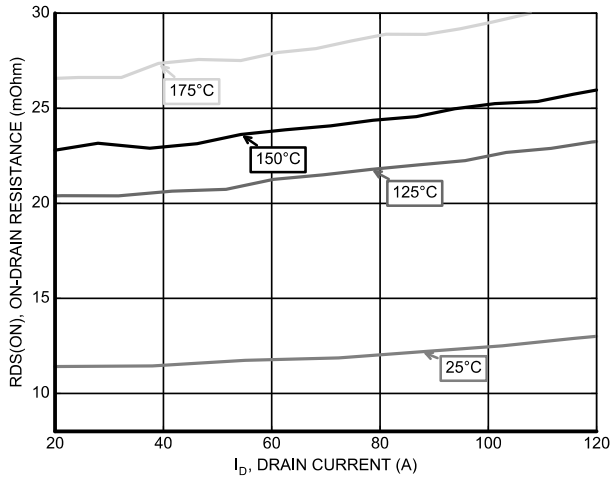


Figure 6. $R_{DS(ON)}$ vs. I_D

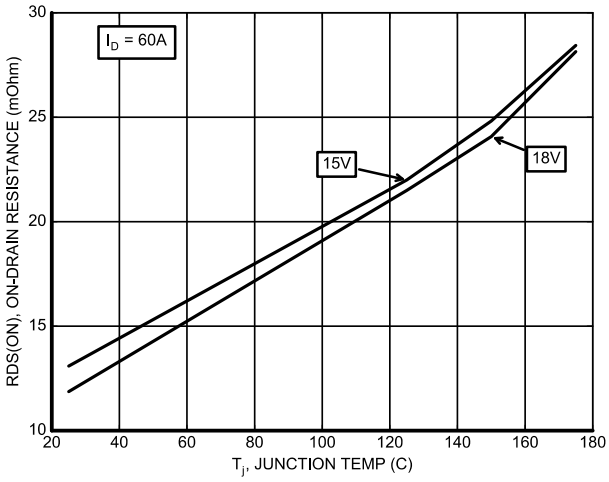


Figure 7. $R_{DS(ON)}$ vs. T_J

TYPICAL CHARACTERISTICS

M1/M2 SIC MOSFET CHARACTERISTIC

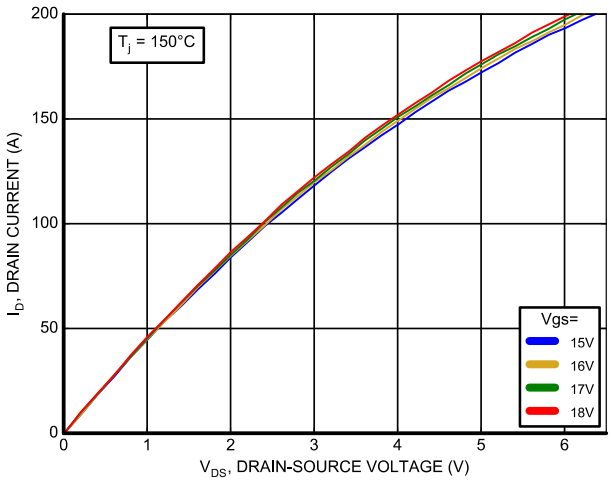


Figure 8. I_D vs. V_{DS}

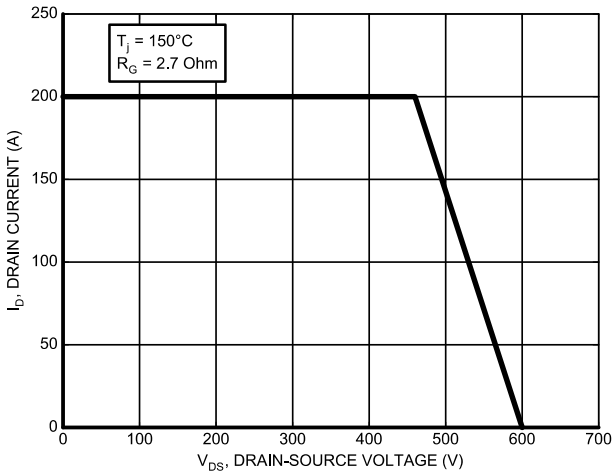


Figure 9. I_D vs. V_{SD}

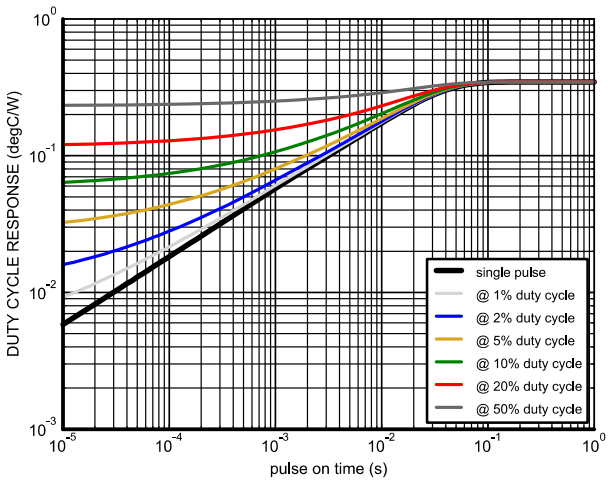


Figure 10. Duty Cycle Response vs. Pulse On Time

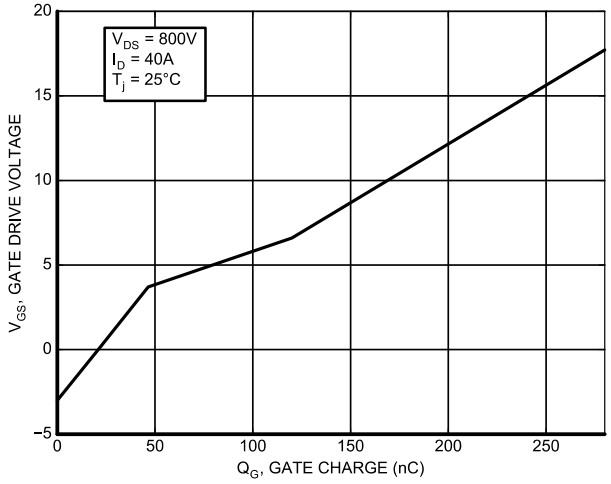


Figure 11. V_{GS} vs. Q_G

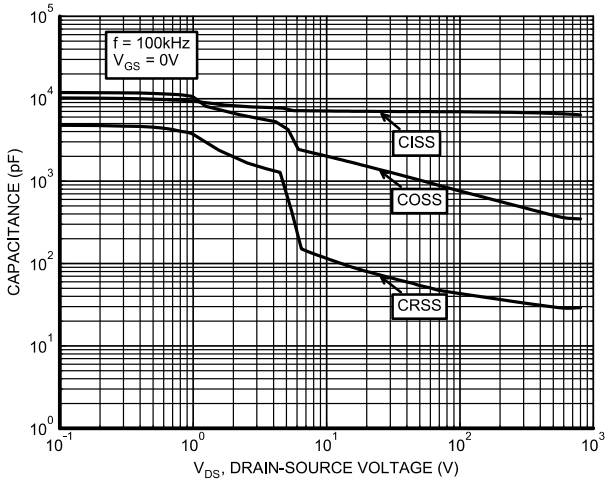


Figure 12. Capacitance vs. V_{DS}

TYPICAL CHARACTERISTICS – HB COMMUTATION PATH

M1/M2 SIC MOSFET SWITCHING CHARACTERISTIC

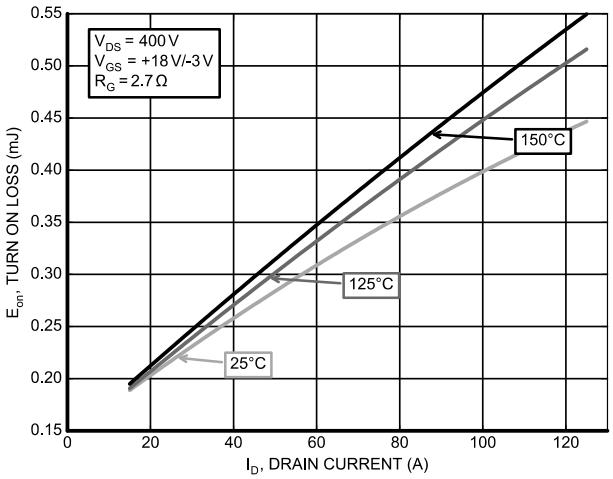


Figure 13. E_{on} vs. I_D

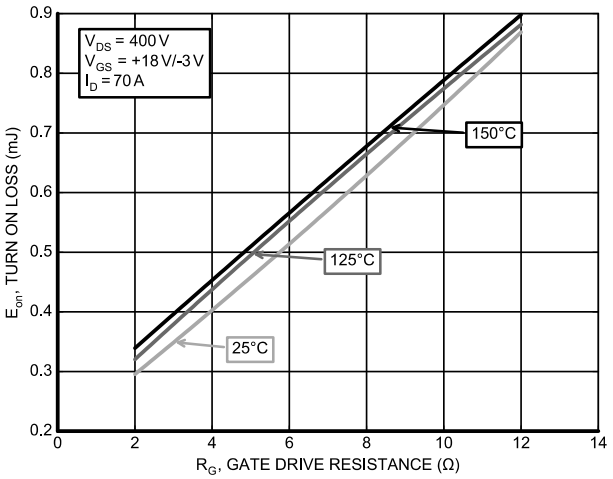


Figure 14. E_{on} vs. R_G

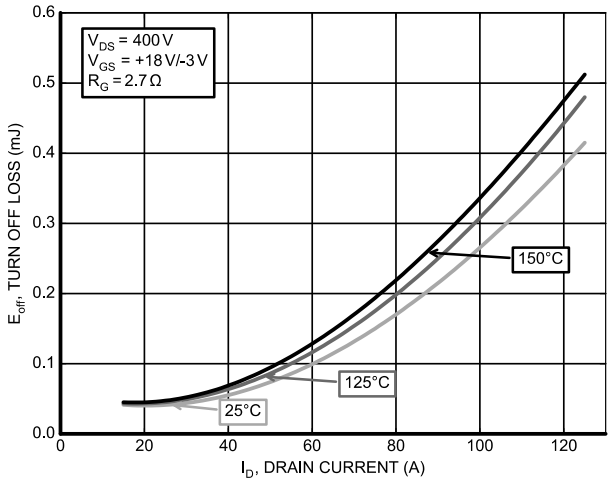


Figure 15. E_{off} vs. I_D

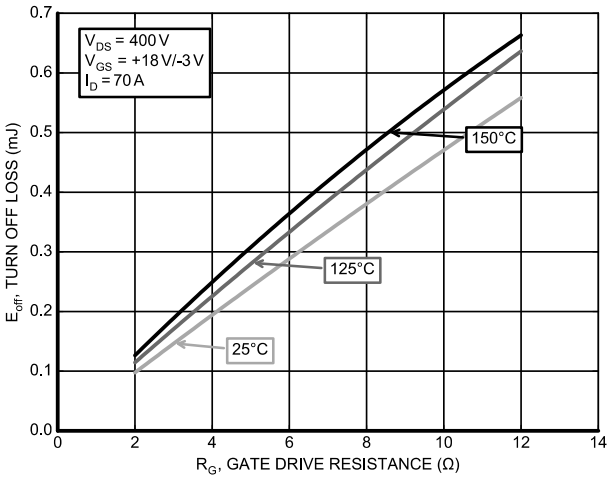


Figure 16. E_{off} vs. R_G

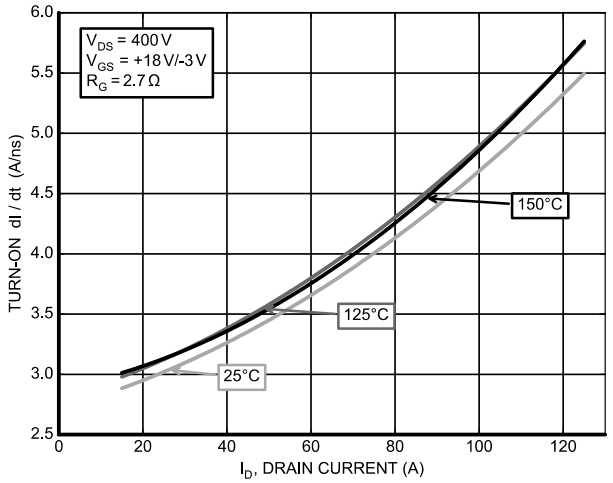


Figure 17. Turn−on dI/dt vs. I_D

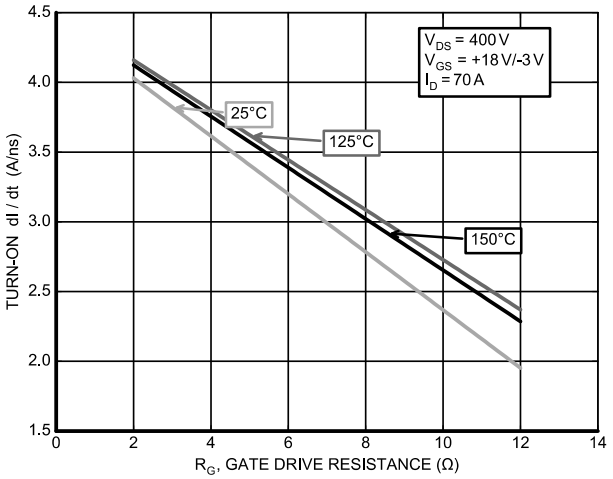


Figure 18. Turn−on dI/dt vs. R_G

TYPICAL CHARACTERISTICS – HB COMMUTATION PATH

M1/M2 SIC MOSFET SWITCHING CHARACTERISTIC

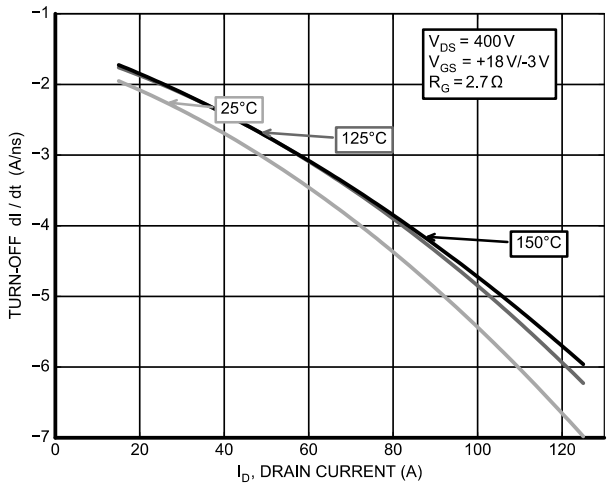


Figure 19. Turn−off dI/dt vs. I_D

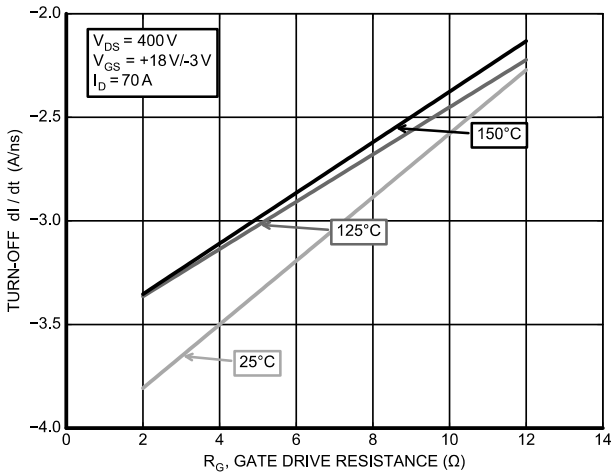


Figure 20. Turn−off dI/dt vs. R_G

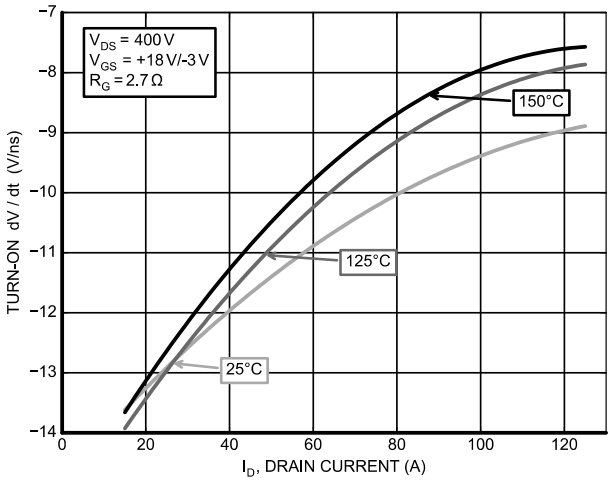


Figure 21. Turn−on dV/dt vs. I_D

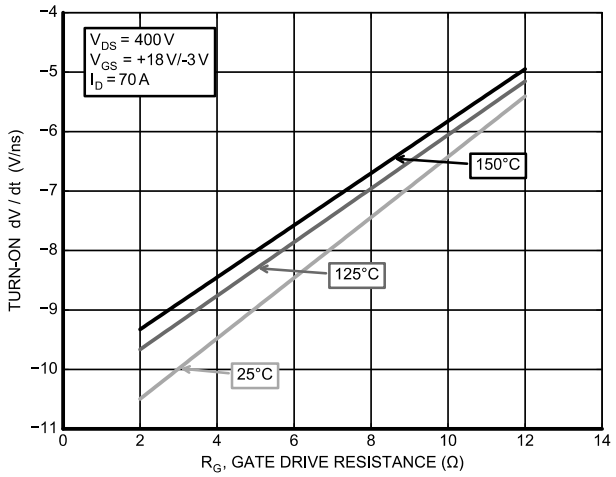


Figure 22. Turn−on dV/dt vs. R_G

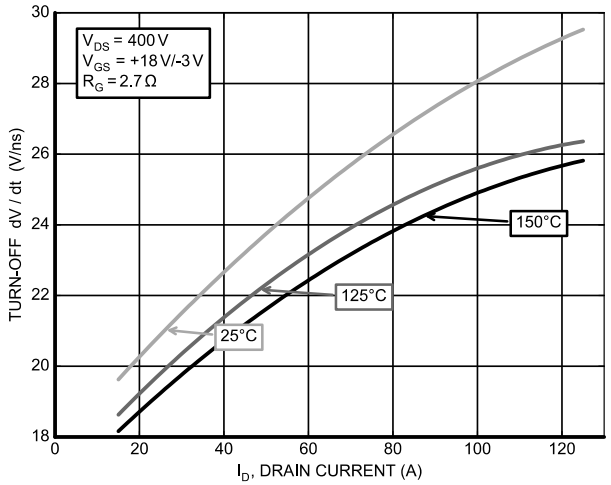


Figure 23. Turn−off dV/dt vs. I_D

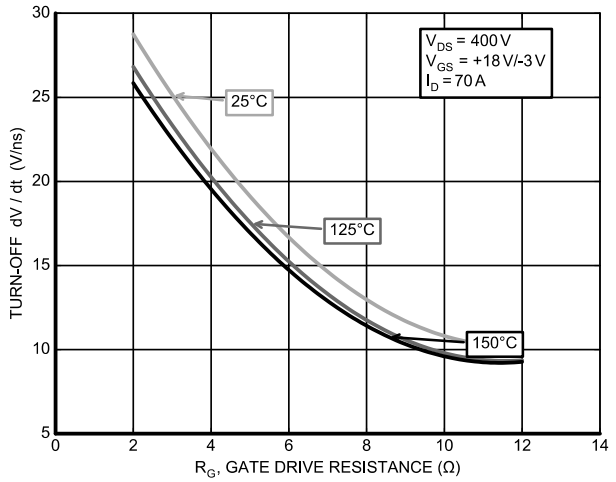


Figure 24. Turn−off dV/dt vs. R_G

TYPICAL CHARACTERISTICS – HB COMMUTATION PATH

M1/M2 SIC MOSFET SWITCHING CHARACTERISTIC

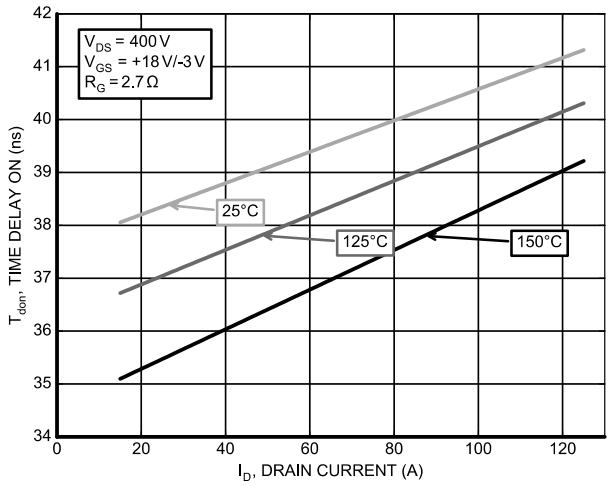


Figure 25. T_{don} vs. I_D

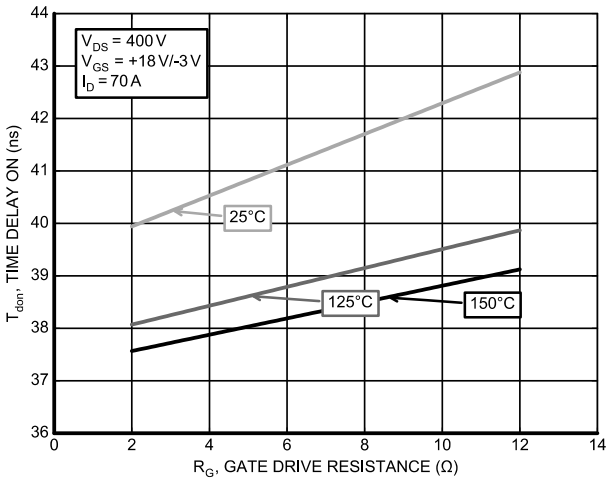


Figure 26. T_{don} vs. R_G

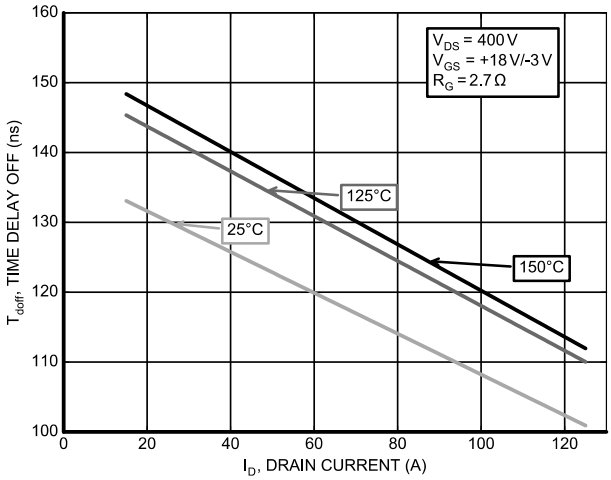


Figure 27. T_{doff} vs. I_D

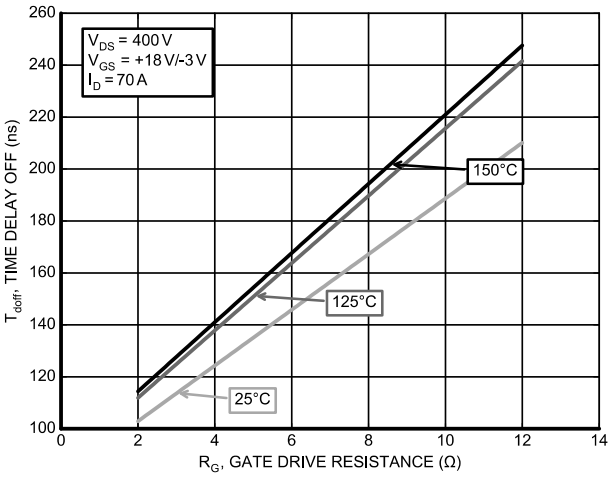


Figure 28. T_{doff} vs. R_G

TYPICAL CHARACTERISTICS – NP COMMUTATION PATH

M1/M2 SIC MOSFET SWITCHING CHARACTERISTIC

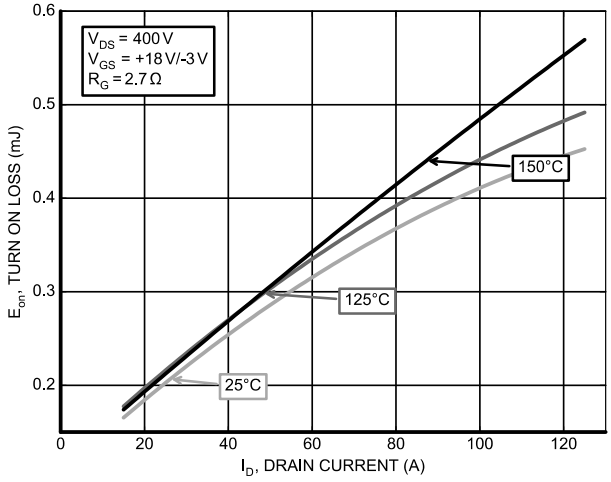


Figure 29. E_{on} vs. I_D

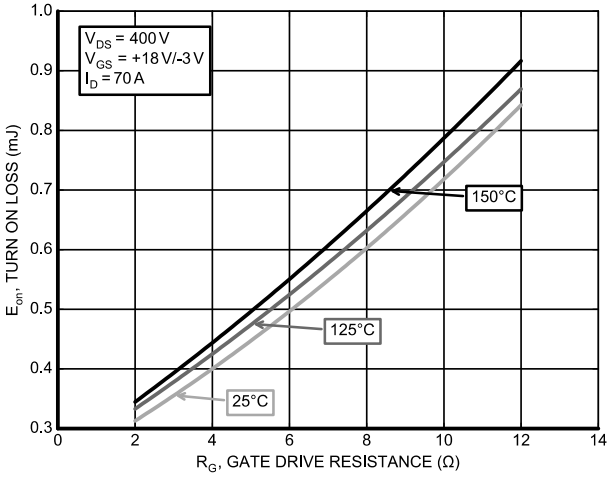


Figure 30. E_{on} vs. R_G

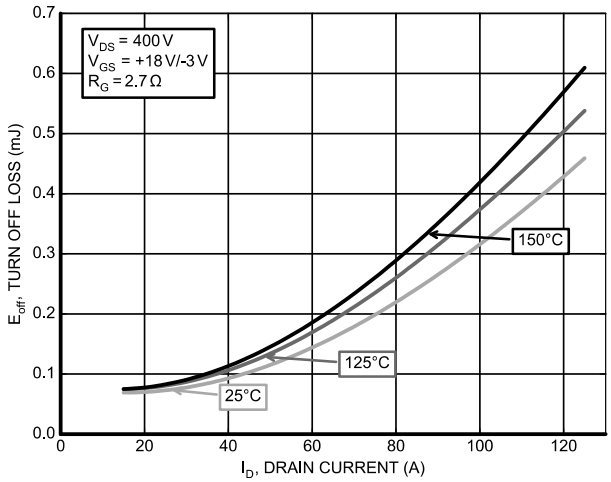


Figure 31. E_{off} vs. I_D

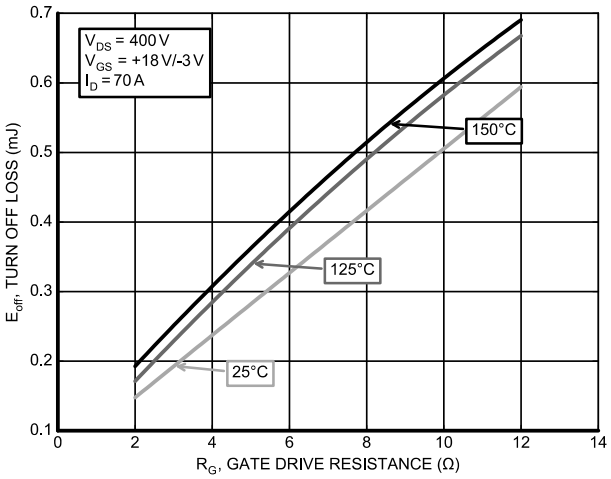


Figure 32. E_{off} vs. R_G

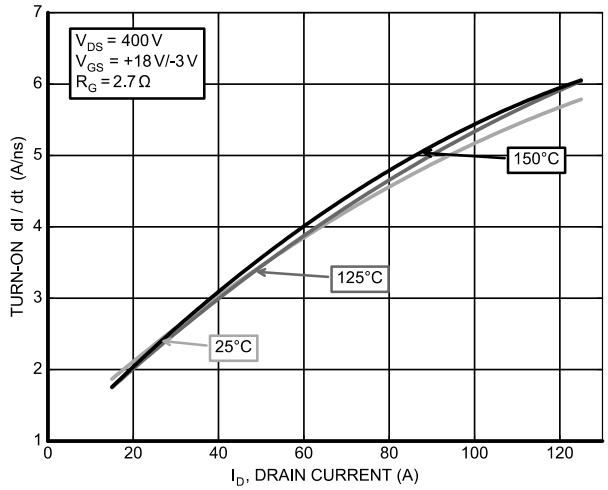


Figure 33. Turn−on dI/dt vs. I_D

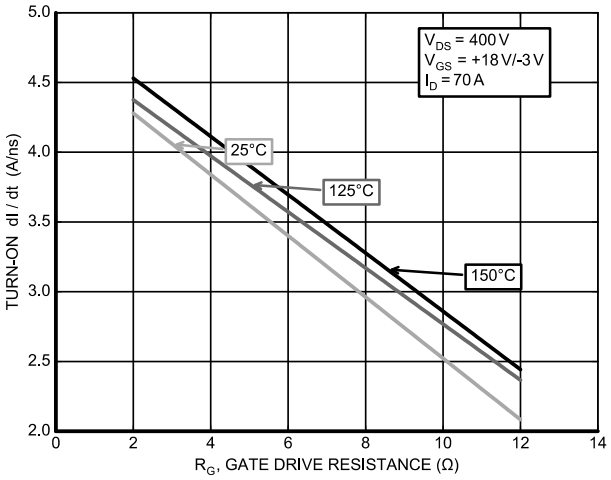


Figure 34. Turn−on dI/dt vs. R_G

TYPICAL CHARACTERISTICS – NP COMMUTATION PATH

M1/M2 SIC MOSFET SWITCHING CHARACTERISTIC

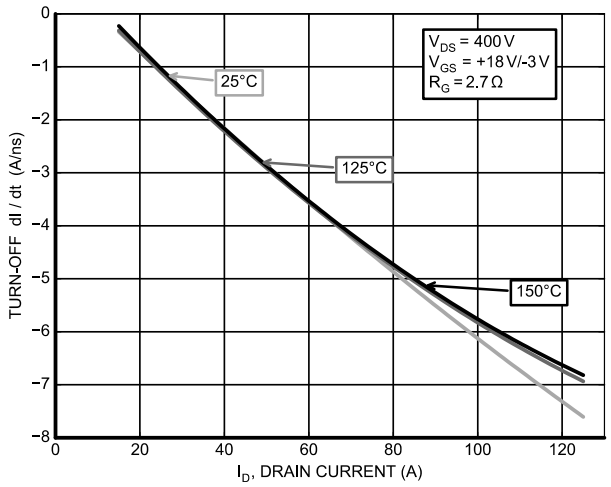


Figure 35. Turn−off dI/dt vs. I_D

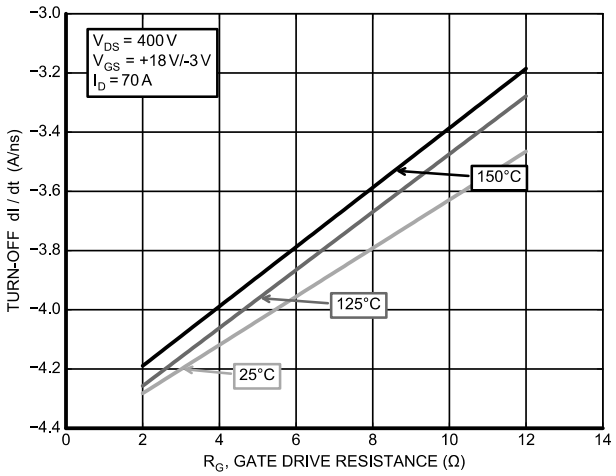


Figure 36. Turn−off dI/dt vs. R_G

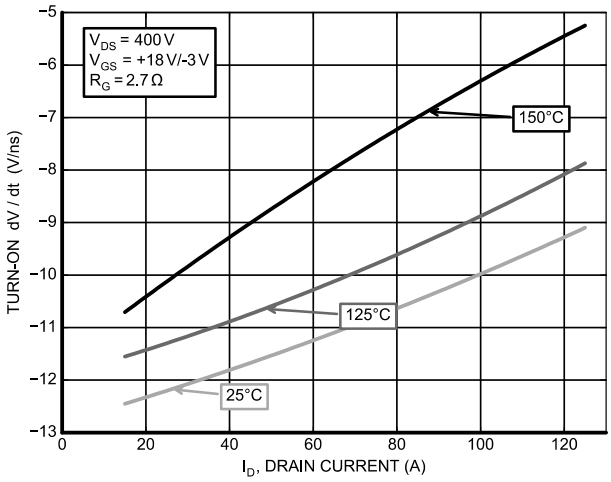


Figure 37. Turn−on dV/dt vs. I_D

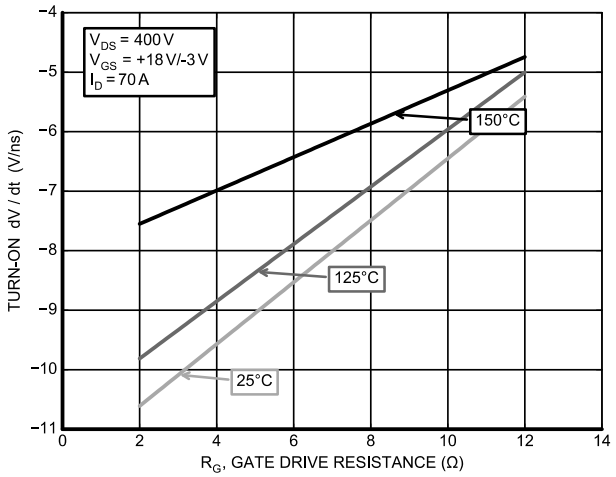


Figure 38. Turn−on dV/dt vs. R_G

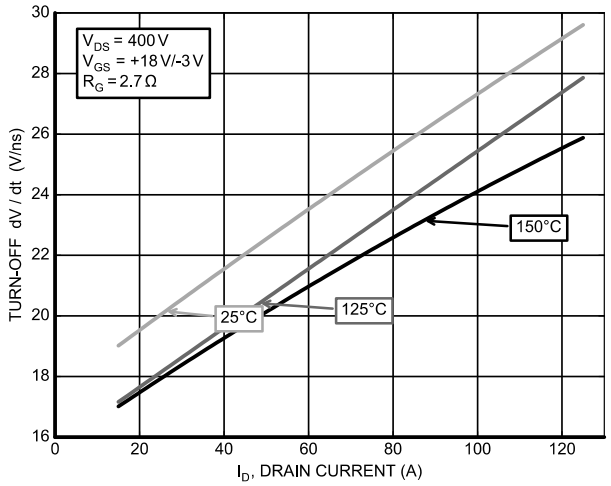


Figure 39. Turn−off dV/dt vs. I_D

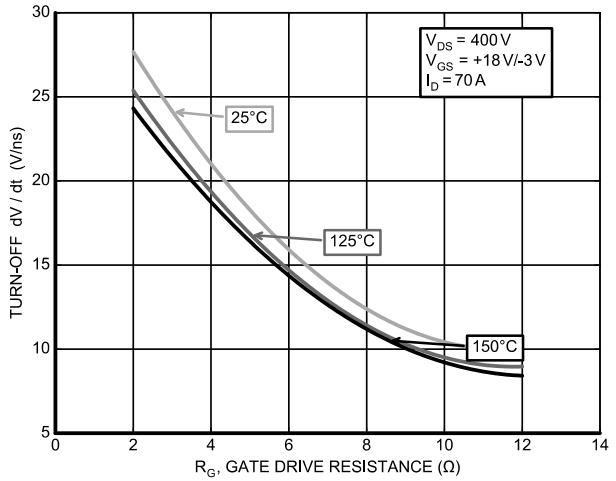


Figure 40. Turn−off dV/dt vs. R_G

TYPICAL CHARACTERISTICS – NP COMMUTATION PATH

M1/M2 SIC MOSFET SWITCHING CHARACTERISTIC

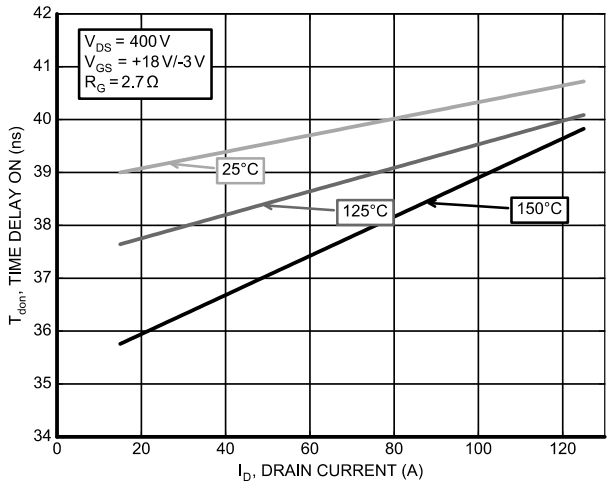


Figure 41. T_{don} vs. I_D

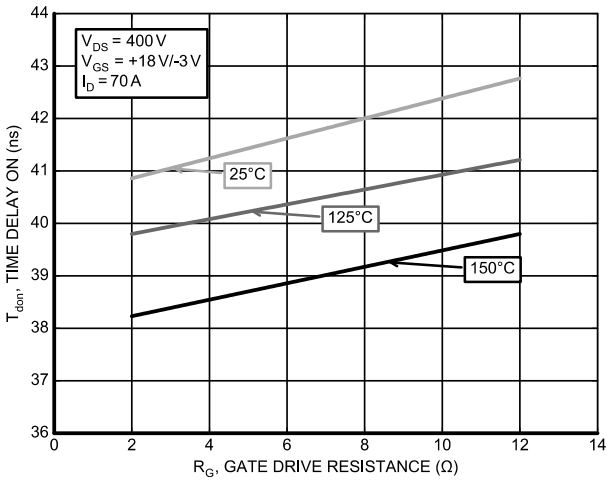


Figure 42. T_{don} vs. R_G

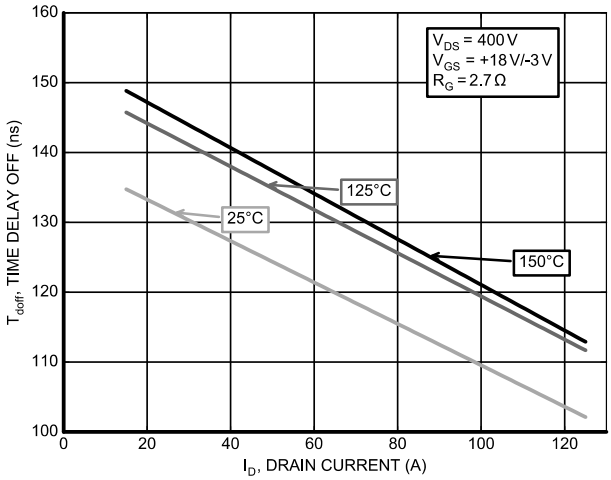


Figure 43. T_{doff} vs. I_D

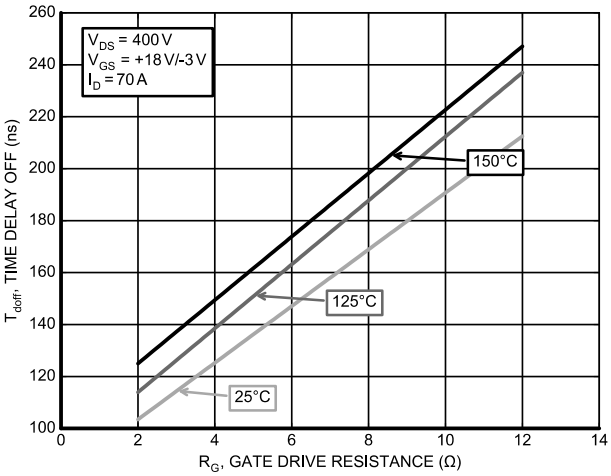


Figure 44. T_{doff} vs. R_G

CAUER NETWORKS – M1, M2

Cauer Element #	M1,2	
	Rth (K/W)	Cth (Ws/K)
1	0.029384	0.005433
2	0.06356	0.016248
3	0.088601	0.038021
4	0.091938	0.034252
5	0.073668	0.078985

FOSTER NETWORKS – M1, M2

Cauer Element #	M1,2	
	Rth (K/W)	Cth (Ws/K)
1	0.014874	0.007783
2	0.018344	0.041519
3	0.016552786	0.081928011
4	0.027204	0.141411
5	0.270176	0.081891

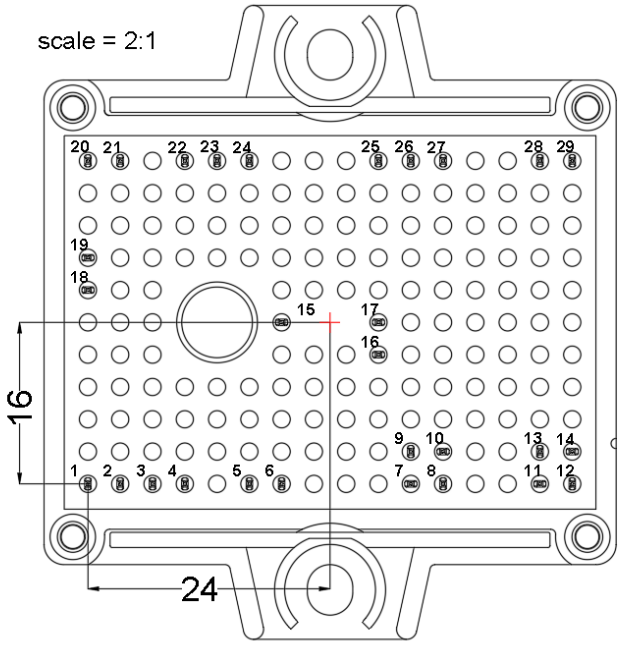


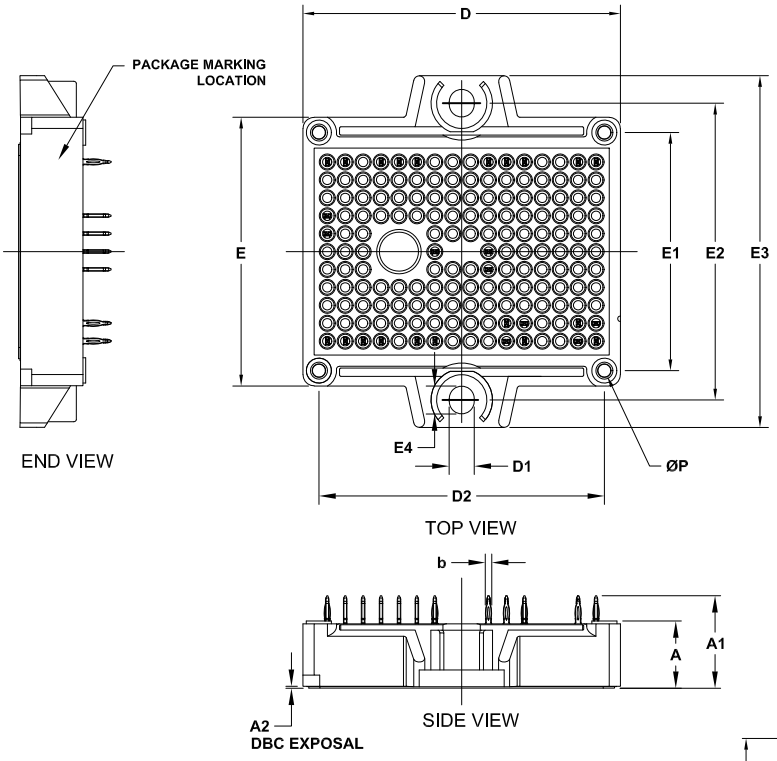
Figure 45. Pin Connections

PIN FUNCTIONS

Pin #	X	Y	Function		Pin #	X	Y	Function
1	0	0	DC−		16	28.8	12.8	G2
2	3.2	0	DC−		17	28.8	16	S2
3	6.4	0	DC−		18	0	19.2	S4
4	9.6	0	DC−		19	0	22.4	G4
5	16	0	G3		20	0	32	TH1
6	19.2	0	S3		21	3.2	32	TH2
7	32	0	N		22	9.6	32	AC
8	35.2	0	N		23	12.8	32	AC
9	32	3.2	N		24	16	32	AC
10	35.2	3.2	N		25	28.8	32	AC
11	44.8	0	DC+		26	32	32	AC
12	48	0	DC+		27	35.2	32	AC
13	44.8	3.2	DC+		28	44.8	32	S1
14	48	3.2	DC+		29	48	32	G1
15	19.2	16	D					

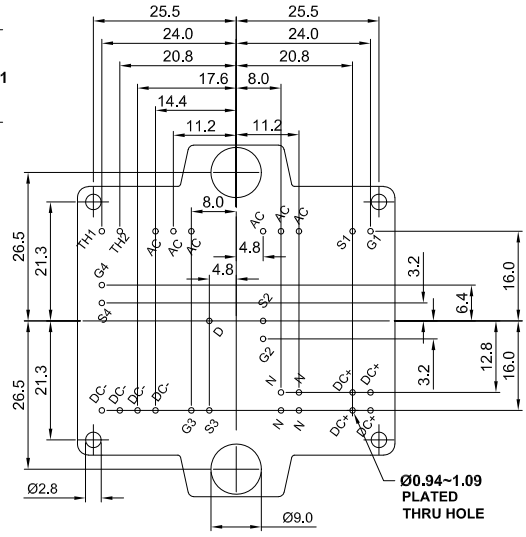
PACKAGE DIMENSIONS

PIM29, 56.7x42.5 (PRESS FIT)
CASE 180HR
ISSUE O



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS ± 0.4mm

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	56.40	56.70	57.00
D1	4.40	4.50	4.60
D2	50.85	51.00	51.15
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



RECOMMENDED MOUNTING PATTERN

* For additional Information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDER RM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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