MOSFET Gate Drive Requirements and Initial Parameter Set Solution with the NCV7544, NCV7546 and NCV7547 Half-bridge Pre-drivers

AND90124/D

Introduction

The NCV7544, NCV7546, and NCV7547 are a family of FLEXMOS™ products for controlling half−bridge connected MOSFETs in automotive actuator applications. These multichannel pre−drivers feature a charge−based gate drive topology that utilizes programmable charge/discharge currents and timers in order to tailor switching performance to a particular MOSFET's gate charge parameters.

This application note describes the various elements of the gate drive topology along with a series of analytical solutions for successful pairing of the pre−driver and MOSFETs while preserving the products' embedded protection and EMI−reducing slope control functionality.

Gate Drive Principle

The gate charge principle is based on the well−known capacitor charge relationship given by

$$Q = C \cdot dv = i \cdot dt \quad \text{(eq. 1)}$$

In practice, a MOSFET's gate input capacitances are charged via programmable currents and timer intervals. The gate charge parameters are obtained directly from the target MOSFET product's datasheet.

The high−side MOSFET's gate charge/discharge is developed in three phases as shown in Figure 1:

I. a turn−on (turn−off) pre−charge phase;
II. a turn−on (turn−off) slew phase;
III. a turn−on (turn−off) overdrive phase.

The low−side MOSFET's gate charge/discharge (not shown in the diagram) is developed in a single 'phase'.

The figure is adapted to the familiar idealized total gate−source charge curve as found in MOSFET datasheets, with the orange curve representing the high−side MOSFET's gate voltage V_{GHX} vs. gate charge Q_G and the blue curve representing the high−side MOSFET's source voltage V_{HBX} vs. gate charge Q_G. Because the high−side MOSFET is configured as a (large−signal) source follower, the gate and source voltages are changing together.

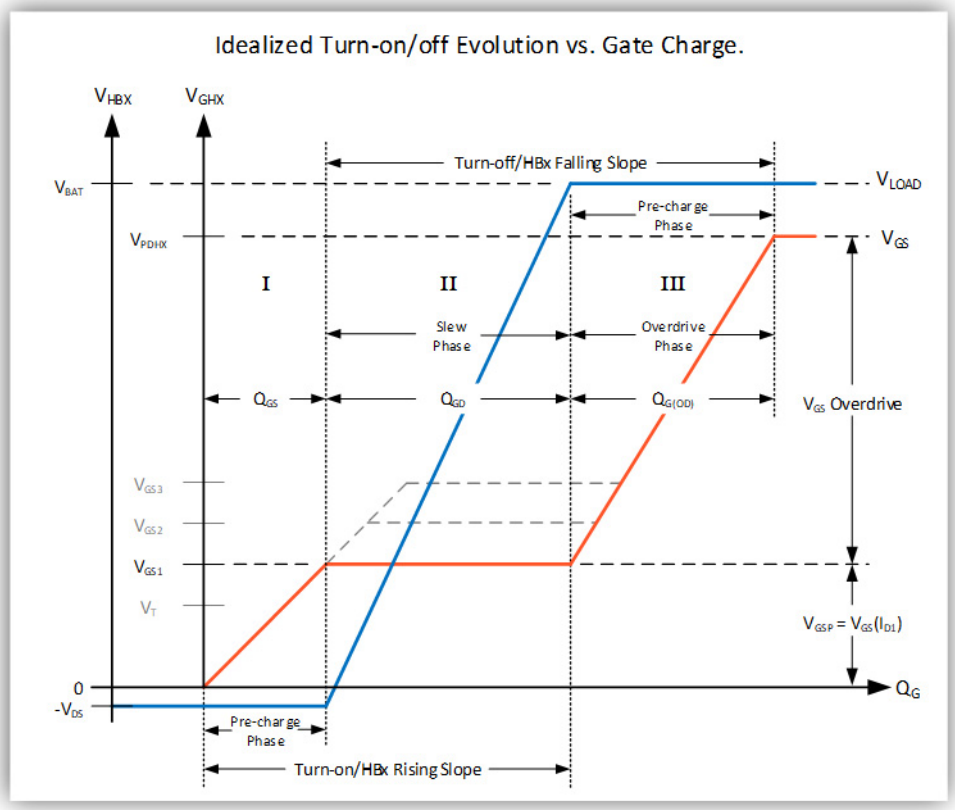

Figure 1. Idealized Gate Charge Evolution

High−side MOSFET Charge

Referring to Figure 1, the high−side MOSFET's gate charge is developed in the following phase sequence.

I. In the turn−on or rising slope pre−charge phase, Q_{GS} is supplied to develop gate voltage to *just below* the value needed to support a particular drain current (e.g. V_{GS1}). Q_{GS} is constructed using one of a range of rising slope pre−charge currents I_{PRCX_R} and timer values t_{PRCX} so that

$$Q_{GS} = I_{PRCX\_R} \times t_{PRCX} \qquad \text{(eq. 2)}$$

The same t_{PRCX} value is used for both the rising and falling pre−charge phases.

II. In the slew phase, Q_{GD} is supplied to increase the gate voltage up to the 'plateau' voltage V_{GS1} where it remains nearly constant with respect to the MOSFET's source as the source voltage rises at a constant rate. A target slope−time value t_{SLEW} − which represents the time required to transition through the plateau − is constructed using the target MOSFET's datasheet Q_{GD} value and one of a range of rising/falling slope currents I_{SRX} so that

$$t_{SLEW} = \frac{Q_{GD}}{I_{SRX}} \qquad \text{(eq. 3)}$$

(Once t_{SLEW} is determined, a dynamic VDS overload detection[1] delay time t_{DLYX} can be selected from a range of values such that $t_{DLYX} > t_{SLEW}$. The same t_{DLYX} value is used for both rising and falling slope dynamic VDS detection delay, and 3x the t_{DLYX} value is used for static VDS detection delay.)

III. In the overdrive phase, the gate continues to be charged via the selected I_{SRX} value up to the drive voltage compliance value of the current source, V_{PDHX}. After a delay time $t_{TIMEOUT}$, the I_{SRX} current is reduced to a steady−state holding current[2] I_{GHX_SS}. The amount of overdrive charge $Q_{G(OD)}$ is determined from the MOSFET datasheet values Q_{GS}, Q_{GD}, and $Q_{G(TOT,\ 10V)}$:

$$Q_{G(OD)} = k_{HS}(Q_{G(TOT,\ 10V)} - Q_{GS} - Q_{GD});$$

$$k_{HS} = \frac{(V_{PDHX} - V_{GS(ID)})}{(10 - V_{GS(ID)})} \qquad \text{(eq. 4)}$$

The time required for the overdrive charge to be accumulated is given by

$$t_{OD\_R} = \frac{Q_{GD(OD)}}{I_{SRX}} \qquad \text{(eq. 5)}$$

1. Not available in the NCV7547 product.
2. The holding current functionality applies only to the high−side pre−driver.

The turn−on time interval $t_{TURN-ON\_HS}$ is comprised of the sum of the time intervals for each phase:

$$t_{TURN-ON\_HS} = t_{PRCX} + t_{SLEW} + t_{OD\_R} = \\ = t_{PRCX} + \frac{1}{I_{SRX}}(Q_{GD} + Q_{GD(OD)}) \quad \text{(eq. 6)}$$

where t_{PRCX} and I_{SRX} are selected from a defined range of values, and t_{SLEW} and t_{OD_R} are dependent upon charge current I_{SRX} and the MOSFET's Q_{GD} and $Q_{GD(OD)}$ gate charge values.

The high−side MOSFET's gate discharge is developed by reversing the sequence of gate charge phases.

III. In the turn−off or falling slope pre−charge phase, $Q_{G(OD)}$ is removed to reduce gate voltage to *just above* the value needed to support a particular drain current (e.g. V_{GS1}). $Q_{G(OD)}$ is constructed using one of a range of falling slope pre−charge currents I_{PRCX_F} and the same t_{PRCX} value used as for the rising pre−charge phase

$$Q_{G(OD)} = I_{PRCX\_F} \times t_{PRCX} \quad \text{(eq. 7)}$$

II. The falling slope slew phase is ideally identical to the rising slope slew phase. Q_{GD} is removed via the same magnitude of current I_{SRX} at the same rate as the rising slope so that

$$t_{FALL} = t_{RISE} = t_{SLEW} = \frac{Q_{GD}}{I_{SRX}} \quad \text{(eq. 8)}$$

I. In the overdrive phase, the gate continues to be discharged via the selected I_{SRX} value down to the drive voltage compliance limit of the current sink. The amount of turn−off overdrive charge to be removed is the same Q_{GS} as supplied in the turn−on pre−charge phase. so the time required for the remaining charge to be removed is

$$t_{OD\_F} = \frac{Q_{GS}}{I_{SRX}} \quad \text{(eq. 9)}$$

The turn−off time interval $t_{TURN-OFF\_HS}$ is comprised of the sum of the time intervals for each phase:

$$t_{TURN-OFF\_HS} = t_{PRCX} + t_{SLEW} + t_{OD\_F} = \\ = t_{PRCX} + \frac{1}{I_{SRX}}(Q_{GD} + Q_{GS}) \quad \text{(eq. 10)}$$

where t_{PRCX} and I_{SRX} are the same values as selected for the rising slope, and t_{SLEW} and t_{OD_R} are dependent upon charge current I_{SRX} and the MOSFET's Q_{GD} and Q_{GDS} gate charge values.

The overall timing and drive current selections t_{PRCX}, t_{DLYX}, I_{PRCX_R}, and I_{SRX} must be chosen carefully in order to optimize switching slope vs. MOSFET switching power vs. EMI trade−offs and to prevent false dynamic VDS overload detection events. The turn−on and turn off pre−charge selections should be chosen to avoid ΔQ_{GS} overshoot at turn−on in order to minimize EMI, and to avoid ΔQ_{GD} undershoot at turn−off to prevent shoot−through with the low−side MOSFET.

Low−side MOSFET Charge

The low−side MOSFET's gate charge and discharge phase is developed via a 4x multiple of the same value of slew current I_{SRX} as is chosen for the high−side slew phase. The turn−on and turn−off time intervals are determined by the I_{SRX} current and the MOSFET's total gate charge so that

$$t_{ON\,|\,OFF\_LS} = \frac{k_{LS} \times Q_{G(TOT,\,10V)}}{4 \times I_{SRX}},$$

$$k_{LS} = \frac{(V_{PDLX} - V_{GS(ID)})}{(10 - V_{GS(ID)})} \quad \text{(eq. 11)}$$

where V_{PDLX} is the drive voltage compliance value of the low−side current source/sink.

PWM Input Deglitch

The high−side and low−side MOSFET switching can be done via SPI or can be synchronized to an external signal via PWMx inputs as shown in Figure 2 below. When switching via PWM, an adaptive de−glitch buffer is used to:

- synchronize the external signal to the logic core clock;
- de−glitch the signal using combinations of the selected t_{BLANKX}, t_{PRCX}, and t_{DLYX} timer values

Two types of adaptive de−glitch are provided, with the ‘type 2’ scheme resulting in a shorter t_{PWM_DGL2} time to facilitate duty ratios closer to 100% in some cases. With either de−glitch type, a state change at the PWMx input must be maintained for at least as long as the t_{PWM_DGL} time in order for the change to be propagated to the gate pre−driver.

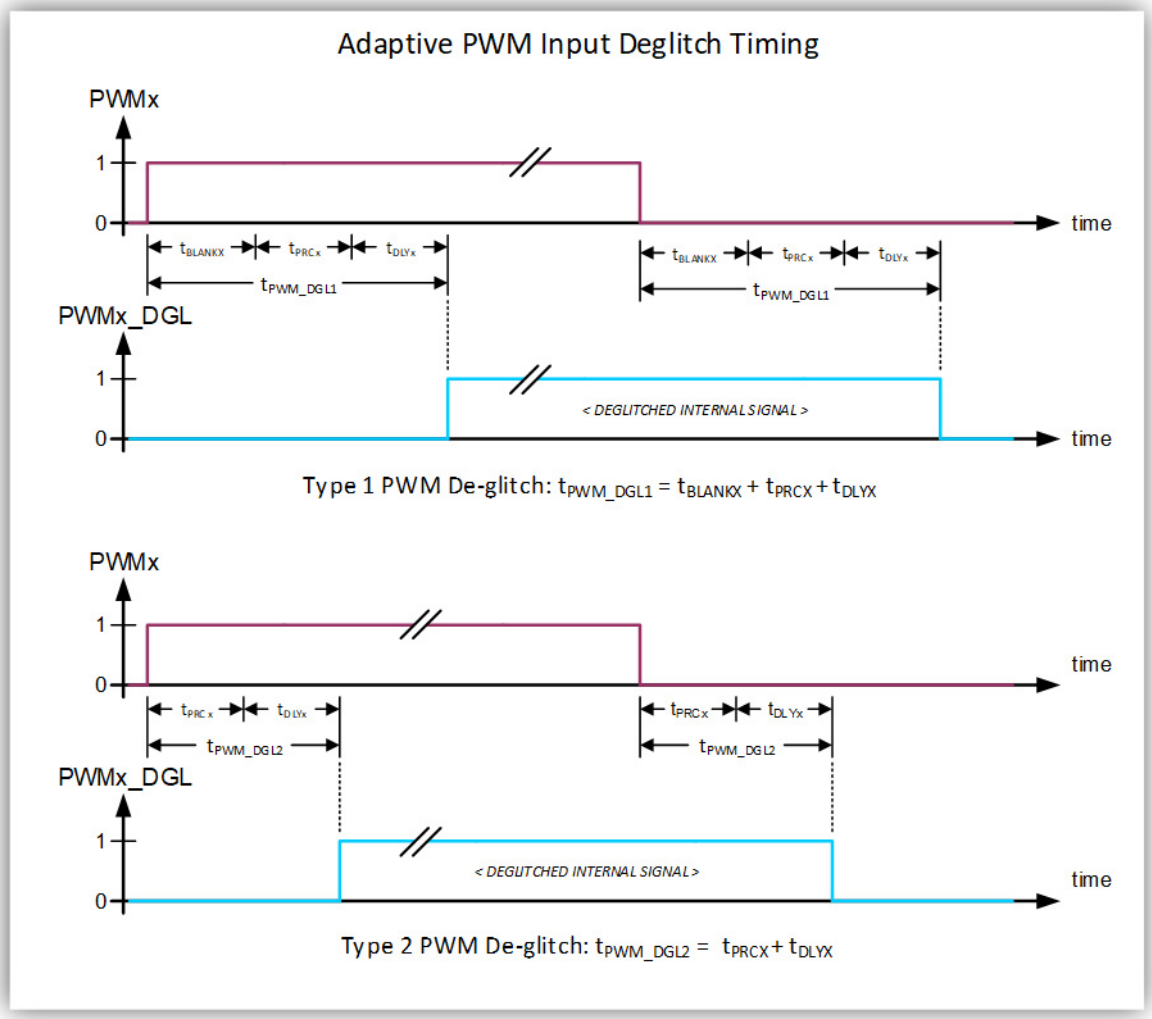

Figure 2. Adaptive De−glitch Timing− Type 1 and Type 2

Timing Constraints

The evolution of the high−side or low−side gate charge/discharge sequence is synchronized to either the SPI signal path or the PWMx input signal path. While each path has propagation delays, the PWM signal path is used when controlling the average voltage at the HBx switching node, so analysis of the PWM signal path delay and the resulting timing constraints are considered next.

In Figure 3 below, I(GHX) or I(GLx) charge/turn−on currents prefixed with '−' are sourced out of the GHx or GLx pin and shown in red. Discharge/turn−off sink currents are prefixed with '+' are shown in green.

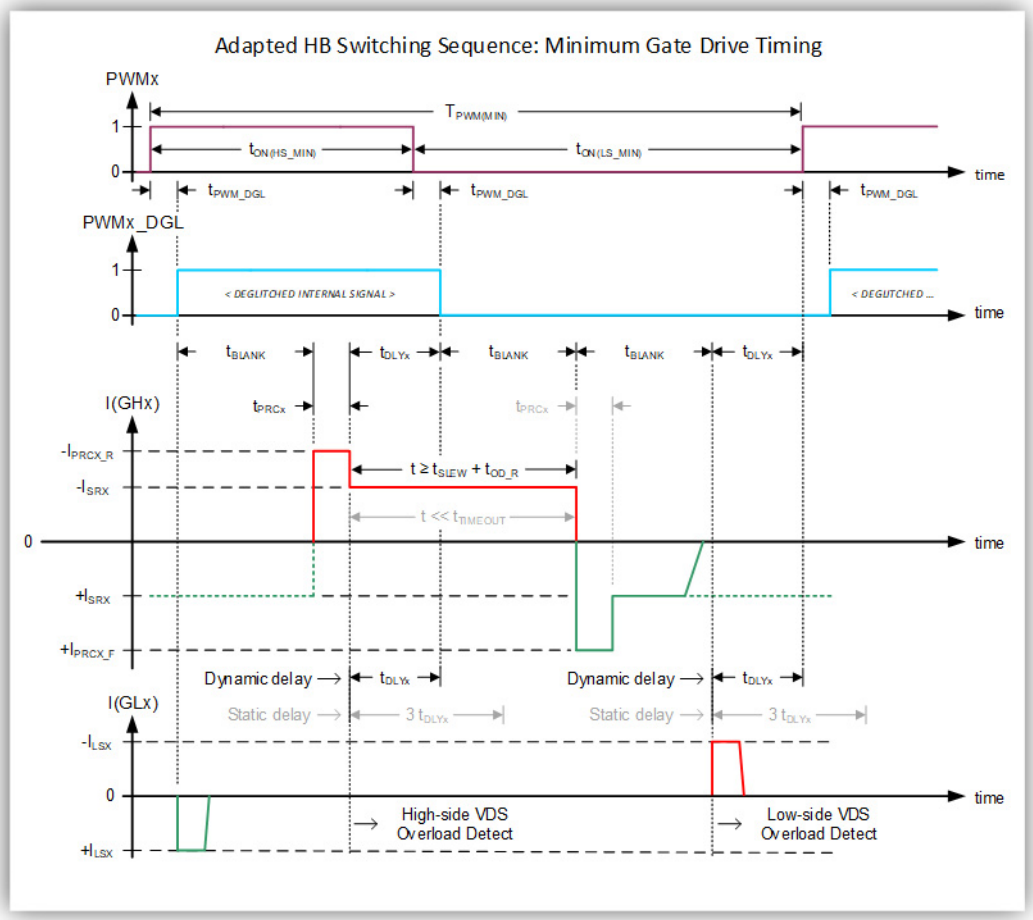

Figure 3. Adapted Internal Gate Drive Timing

Low−side Turn−off, High−side Turn−on

Referring to Figure 3, turn−off of the low−side gate drive is synchronized to the de−glitched internal signal PWMx_DGL and begins at the rising edge of PWMx_DGL where a non−overlap timer t_{BLANK} is started. The expectation is that the low−side MOSFET's gate will be fully discharged *before* turn−on of the high−side MOSFET begins at the end of the t_{BLANK} interval. The same value selected for t_{BLANK} is used for all relevant t_{BLANK} timing intervals shown in the diagram.

Turn−on of the high−side gate drive begins at the end of the t_{BLANK} time interval where the high−side MOSFET pre−charge timer t_{PRCX} is started along with the $t_{TIMEOUT}$ limit timer. The same value selected for t_{PRCX} is used for all relevant t_{PRCX} timing intervals.

At the end of the pre−charge interval, the high−side VDS overload dynamic and static blanking detect timers, t_{DLYX} and 3 t_{DLYX} respectively, are started along with slew current I_{SRX}. The same values selected for t_{DLYX} and for I_{SRX} are used for all relevant t_{DLYX} and I_{SRX} (t_{SLEW}) timing intervals.

The dynamic and static blanking timers run concurrently, but the dynamic blanking timer is the focus in this analysis because the expectation is that the slew phase is completed *before* the end of the dynamic VDS blanking interval so that

$$t_{DLYX} > t_{SLEW} \qquad \text{(eq. 12)}$$

This result makes clear that the value of t_{DLYX} chosen for the dynamic VDS blanking interval is dependent upon the selected value slew current I_{SRX} and the MOSFET's gate−drain charge Q_{GD}. The requirement of equation 12 ensures that the dynamic overload detection function is preserved.

While the PWMx_DGL signal remains in the ‘1’ state, overdrive charge $Q_{G(OD)}$ continues to accumulate via the selected I_{SRX} value. Since the falling slope/turn−off pre−charge current I_{PRC_F} is chosen to deplete the accumulated overdrive charge, the minimum high−side ‘ON’ time needs to account for this condition by replacing t_{DLYX} with $t_{SLEW} + t_{OD\_R}$. If this is not accounted for, the turn−off pre−charge current will be much larger than that required to deplete the lower accumulated charge if ‘ON’ time is constructed instead using t_{DLYX}, and the turn−off slope can be abrupt due to pre−charge overshoot.

The previously defined turn−on time interval $t_{TURN-ON\_HS}$ (Equation 6) is modified here to include the t_{BLANK} interval so that the minimum high−side ‘ON’ time $t_{ON(MIN\_HS)}$ is defined as

$$t_{ON(MIN\_HS)} = t_{BLANK} + t_{PRCX} + t_{SLEW} + t_{OD\_R} \quad \text{(eq. 13)}$$

High−side Turn−off, Low−side Turn−on

Turn−off of the high−side gate drive begins at the falling edge of PWMx_DGL where a first t_{BLANK} time interval is started. This first blanking interval provides symmetry with respect to the rising and falling edges of the PWMx_DGL signal.

At the end of the first blanking interval, the high−side pre−charge t_{PRCX} time interval is started along with a second t_{BLANK} non−overlap time interval. The expectation is that the high−side MOSFET’s gate will be fully discharged *before* turn−on of the low−side MOSFET begins at the end of the *second* t_{BLANK} interval so that at *turn−off* of the high−side (refer to Figure 3) we have $Q_{G(OD)} = Q_{GS}$ so that

$$t_{BLANK} > t_{TURN-OFF\_HS} > t_{PRCX} + \frac{(Q_{GD} + Q_{GS})}{I_{SRX}} \quad \text{(eq. 14)}$$

This result makes clear that the value of t_{BLANK} chosen for the non−overlap blanking interval is dependent upon the selected rising/falling pre−charge time interval t_{PRCX} plus the time interval $t_{TURN-OFF\_HS}$ (Equation 10) required to deplete the remaining gate charge, which is dependent upon the I_{SRX}, Q_{GD}, and Q_{GS} values.

At the end of the second blanking interval, the low−side dynamic VDS overload time interval t_{DLYX} is started. The expectation is that the low−side turn−on is completed *before* the end of the t_{DLYX} interval (previously dimensioned according to the slew current I_{SRX} as selected to satisfy the high−side turn−on requirements) such that the following condition $t_{DLYX} > t_{ON|OFF\_LS}$ (Equation 11) is satisfied for the low−side MOSFET:

$$t_{DLYX} > \frac{k_{LS} \times Q_{G(TOT,\ 10V)}}{4 \times I_{SRX}} \quad \text{(eq. 15)}$$

Since the low−side drive current is 4 times the selected I_{SRX} value, it is assured that the low−side MOSFET will be fully on by the end of the t_{DLYX} interval, assuming the same MOSFET types are used for both high−side and low−side switches. The minimum low−side ‘ON’ time $t_{ON(MIN\_LS)}$ is defined as

$$t_{ON(MIN\_LS)} = 2 \times t_{BLANK} + t_{DLYX} \quad \text{(eq. 16)}$$

PWM Limitations

When all of the gate drive parameters (t_{PRCX}, I_{PRCX_R}, I_{PRCX_F}, I_{SRX}, t_{DLYX}, t_{BLANKX}) have been selected, an estimate of the allowable PWM frequency and duty ratios can be made. PWM limitations based on timing requirements and charge pump loading include:

- the type of adaptive de−glitch selected and the resulting t_{PWM_DGL} value;
- the minimum high−side and low−side ‘ON’ time intervals, $t_{ON(MIN\_HS)}$ and $t_{ON(MIN\_LS)}$ respectively;
- the capability of the particular pre−driver product’s charge pump.

Construction of the PWM period is as shown in Figure 4.

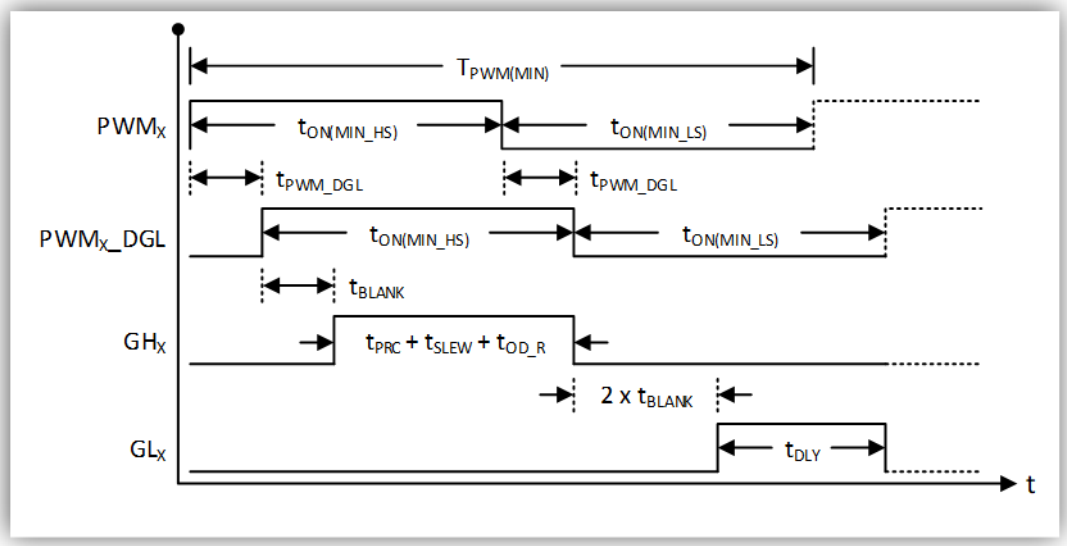

Figure 4. PWM Period Construction

The de−glitched input signal PWMx_DGL is comprised of combinations of the same t_{BLANKX}, t_{PRCX}, and t_{DLYX} timer values that are used for constructing the respective high−side and low−side ‘ON’ time intervals.

A state change at the PWMx input must be maintained for at least as long as the t_{PWM_DGL} time in order for that change to be propagated internally to the gate pre−driver. For either $t_{ON(MIN\_HS)}$ or $t_{ON(MIN\_LS)}$, and for both t_{PWM_DGL1} and t_{PWM_DGL2} de−glitch types, this leads to the boundary condition requirement

$$t_{ON(MIN\_HS|LS)} > t_{PWM\_DGL} \quad \text{(eq. 17)}$$

In a half−bridge topology, energy is delivered to the load during the high−side MOSFET ‘ON’ time, and energy is (actively) recirculated in the load during the low−side MOSFET ‘ON’ time. The achievable duty ratio ‘D’ with frequency $f_{PWM(MAX)} = 1/T_{PWM(MIN)}$ is determined with respect to the high−side ‘ON’ time via the minimum high−side ‘ON’ time and minimum low−side ‘ON’ time values:

$$f_{PWM(MAX)} \times t_{ON(MIN\_HS)} \le D \le 1 - (f_{PWM(MAX)} \times t_{ON(MIN\_LS)}) \quad \text{(eq. 18)}$$

Using $t_{ON(MIN\_HS)}$ to set the lower duty ratio bound ensures that the minimum high−side ‘ON’ time is satisfied, while using $t_{ON(MIN\_LS)}$ to set the upper duty ratio bound ensures that the minimum low−side ‘ON’ time is satisfied.

Referring to Figure 4, it can be seen that each of the internal high−side GHx and low−side GLx signals are delayed by a multiple of the t_{BLANK} blanking time interval. The delay, which is needed in order to prevent a shoot−through (or cross−conduction) hazard between the high−side and low−side MOSFETs, imposes a further set of boundary condition requirements:

$$D_{(MIN)} \ge f_{PWM} \times t_{BLANK} \quad \text{(eq. 19)}$$

$$D_{(MAX)} \le 1 - (f_{PWM} \times 2 \times t_{BLANK}) \quad \text{(eq. 20)}$$

The first requirement of equation 19 must be met for the high−side MOSFET to just begin its turn−on sequence while the second requirement of equation 20 must be similarly met for the low−side MOSFET to just begin its turn−on sequence. Failure to meet the first requirement will result in no energy being delivered to the load. Failure to meet the second requirement will result in stored load energy being passively recirculated in the low−side MOSFET’s body diode instead of the active $R_{DS(ON)}$ of its channel resistance which can result in increased power dissipation.

Charge Pump Loading

In addition to the PWM timing requirements, charge pump loading needs to be considered so that the charge pump’s capability is not exceeded. An analysis based on energy stored in a capacitor provides an estimate of the total steady−state average gate charge $Q_{G(TOT\_SS)}$ the charge pump could support[3]:

$$Q_{G(TOT\_SS)} = 2 \times \left(\frac{I_{CP(DC)} - I_{DC}}{f_{PWM}} \right) \quad \text{(eq. 21)}$$

where I_{DC} is any static loading current (e.g. bleed resistances etc.), and $I_{CP(DC)}$ is the steady−state charge pump current specified in the pre−driver product’s datasheet. The PWM frequency may be the datasheet recommended maximum value (25 kHz) or any lower target value.

Pre−driver Parameter Solution Example

The following worked example is offered as a method for constructing a pre−driver and target MOSFET initial parameter solution set. The method is applicable to each of the NCV7544/46/47 family devices. An **onsemi** NVMFS5C460NL 40 V/4.5 mΩ/78 A logic−level device is chosen as a target MOSFET for the example.

A table of gate parameters (Figure 5) and a total gate charge curve (Figure 6) from the NVMFS5C460NL[4] datasheet are shown below.

CHARGES, CAPACITANCES & GATE RESISTANCE			NVMFS5C460NL			
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V		1300		pF
Output Capacitance	C_{OSS}			530		
Reverse Transfer Capacitance	C_{RSS}			22		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 35 A		23		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 35 A		11		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.5		
Gate−to−Source Charge	Q_{GS}			4.7		
Gate−to−Drain Charge	Q_{GD}			3.0		
Plateau Voltage	V_{GP}			3.3		V

Figure 5. NVMFS5C460NL Datasheet – MOSFET Gate Parameters

3. Since the analysis goal is to determine the steady state gate charge supplied by the charge pump, discharge of the gate is not considered here.
4. **onsemi** product datasheet publication order number NVMFS5C460NL/D, February, 2017 − Rev. 2

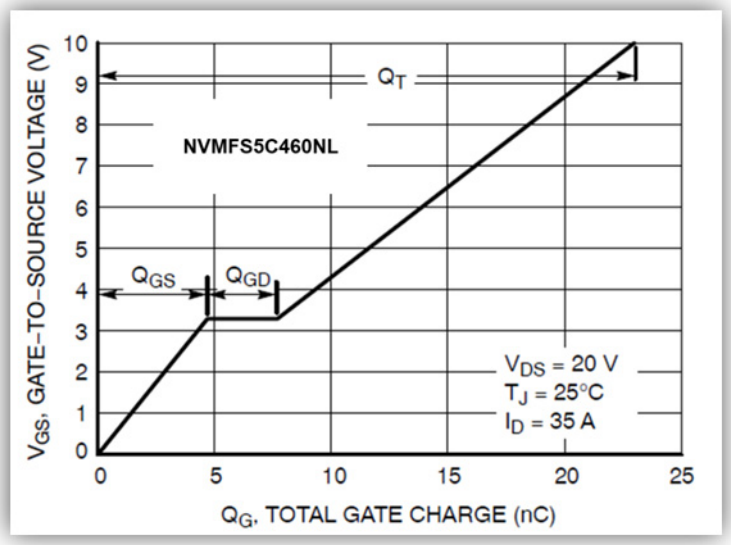

Figure 6. NVMFS5C460NL Datasheet – MOSFET Total Gate Charge Curve

The MOSFET's gate charge parameters Q_{GS}, Q_{GD}, and $Q_{G(TOT)}$ at V_{GS} = 10 V will be used for the solution. The gate charge curve characterizes typical device behavior at the particular operating point as given for the gate charge parameters – i.e. V_{GS} = 10 V, V_{DS} = 20 V, and I_D = 35 A. Other operating points will result in different values for the gate charges since Q_{GS} will vary with I_D as $V_{GS(ID)}$ varies, while Q_{GD} and $Q_{G(TOT)}$ will vary as V_{DS} varies. An assumed slew time t_{SLEW} = 1 μs will be targeted. The example solutions assume nominal conditions and do not take into account component tolerances or environment effects.

Rising and Falling Pre−charge Solutions

The rising pre−charge requirement Q_{PRC_R} is taken directly from the MOSFET datasheet Q_{GS} value and applied to equation 2:

$$Q_{PRC\_R} = Q_{GS} = I_{PRCX\_R} \times t_{PRCX} = 4.7\ nC$$

The falling pre−charge requirement Q_{PRC_F} is evaluated via equation 4. The values $Q_{G(TOT,\ 10V)}$, Q_{GS}, Q_{GD}, and $V_{GS(ID)} = V_{GP}$ are taken directly from the MOSFET datasheet, and the V_{PDHX} value directly from the pre−driver datasheet giving

$$Q_{G(OD)} = \frac{(8.9 - 3.3)\ V}{(10 - 3.3)\ V} \times (23 - 4.7 - 3.0)\ nC = 12.8\ nC$$

Applying this result to equation 7 gives

$$Q_{PRC\_F} = Q_{QG(OD)} = I_{PRCX\_F} \times t_{PRCX} = 12.8\ nC$$

Both the rising and falling pre−charge phases use the same time interval t_{PRCX} while suitable values for the charge and discharge currents need to be selected to match the target MOSFET's respective Q_{GS} and $Q_{G(OD)}$ requirements without significant overshoot or undershoot.

The pre−driver products' datasheets provide the available pre−charge time and current parameters, which are used to construct pre−charge solutions from the following tables for each of the rising slope (Table 1, Q_{PRC_R} = 4.7 nC) and falling slope (Table 2, Q_{PRC_F} = 12.8 nC) targets.

Table 1. RISING SLOPE PRE−CHARGE SOLUTIONS

	Pre−charge Rise Current I_{PRC_R} (mA): I_PCRx[2:0]							
	1.50	5.25	8.63	12.38	16.50	20.25	24.00	28.13
t_{PRC} (ns)	Turn−on/Rise Pre−charge Q_{PRC_R} (nC)							
100	0.15	0.53	0.86	1.24	1.65	2.03	2.40	2.81
200	0.30	1.05	1.73	2.48	3.30	4.05	4.80	5.63
300	0.45	1.58	2.59	3.71	4.95	6.08	7.20	8.44
400	0.60	2.10	3.45	4.95	6.60	8.10	9.60	11.25

Table 2. FALLING SLOPE PRE−CHARGE SOLUTIONS

	Pre−charge Fall Current I_{PRC_F} (mA): I_PCFx[2:0]							
	28.88	35.63	42.00	48.38	55.13	61.50	67.88	74.63
t_{PRC} (ns)	Turn−off/Fall Pre−charge Fall Q_{PRC_F} (nC)							
100	2.89	3.56	4.20	4.84	5.51	6.15	6.79	7.46
200	5.78	7.13	8.40	9.68	11.03	12.30	13.58	14.93
300	8.66	10.69	12.60	14.51	16.54	18.45	20.36	22.39
400	11.55	14.25	16.80	19.35	22.05	24.60	27.15	29.85

Two potential solutions for each of the rising/falling pre−charge intervals are selected from the tables (shaded cells):

1. rising slope pre−charge, target Q_{GS} = 4.7 nC:
   a. t_{PRCX} = 200 ns, I_{PRC_R} = 24.0 mA, Q_{GS} = 4.80 nC
   b. t_{PRCX} = 300 ns, I_{PRC_R} = 16.5 mA, Q_{GS} = 4.95 nC
2. falling slope pre−charge, target $Q_{G(OD)}$ = 12.8 nC:
   a. t_{PRCX} = 200 ns, I_{PRC_F} = 61.5 mA, $Q_{G(OD)}$ = 12.3 nC
   b. t_{PRCX} = 300 ns, I_{PRC_F} = 42.0 mA, $Q_{G(OD)}$ = 12.6 nC

Defining the relative magnitude $\Delta Q_{G(\%)}$ as the ratio of a chosen solution $Q_{G(CHOSEN)}$ value to a target $Q_{G(TARGET)}$ value gives

$$\Delta Q_{G(\%)} = \left(\frac{Q_{G(CHOSEN)}}{Q_{G(TARGET)}} - 1 \right) \times 100\% \qquad \text{(eq. 22)}$$

Evaluating the two rising slope solutions via equation 22 for relative ΔQ_{GS} overshoot (+%) and undershoot (−%) gives

$$\Delta Q_{GS(200ns)} = \frac{4.80}{4.70} - 1 = +2.1\%;$$

$$\Delta Q_{GS(300ns)} = \frac{4.95}{4.70} - 1 = +5.3\%$$

Similarly, evaluating the two falling slope solutions for relative $\Delta Q_{G(OD)}$ overshoot and undershoot gives

$$\Delta Q_{G(OD)(200ns)} = \frac{12.3}{12.8} - 1 = -3.9\%;$$

$$\Delta Q_{G(OD)(300ns)} = \frac{12.6}{12.8} - 1 = -1.6\%$$

Rising and Falling Slew Solution

Any ΔQ_G charge overshoot/surplus or undershoot/deficit will affect the target slew time solution, which is determined by the slew current I_{SRX} and the target MOSFET's datasheet Q_{GD} charge in the 'plateau' region, plus or minus any pre−charge surplus or deficit. Modifying equation 3 accounts for this effect so that

$$t_{SLEW\_R} = \frac{Q_{GD} \pm \Delta Q_{GS}}{I_{SRX}} = \frac{Q_{SLEW\_R}}{I_{SRX}} \qquad \text{(eq. 23)}$$

$$t_{SLEW\_F} = \frac{Q_{GD} \pm \Delta Q_{G(OD)}}{I_{SRX}} = \frac{Q_{SLEW\_F}}{I_{SRX}} \qquad \text{(eq. 24)}$$

The choice of a dynamic VDS overload delay time t_{DLYX} with respect to t_{SLEW} also needs to be considered so that the timing constraint of Equation 12 $t_{DLYX} > t_{SLEW}$ is not violated.

Since a single value for t_{DLYX} applies to both rising and falling slopes, a better choice for a pre−charge solution set is provided via solutions *Q_{GS} = 4.80 nC* (1.a) and *$Q_{G(OD)}$ = 12.3 nC* (2.a) as these are more closely matched in terms of their relative ΔQ_G magnitudes (i.e. +2.1% and −3.9% respectively).

Defining the signed magnitude of ΔQ_G as the difference between the target value $Q_{G(TARGET)}$ and the chosen solution value $Q_{G(CHOSEN)}$ gives

$$\Delta Q_G = Q_{G(TARGET)} - Q_{G(CHOSEN)} \qquad \text{(eq. 25)}$$

Evaluating the numerators of equation 23 and equation 24 with the MOSFET's datasheet target Q_{GD} requirement and the respective ΔQ_G magnitude values as defined via equation 25 yields

$$Q_{SLEW\_R} = Q_{GD} \pm \Delta Q_{GS} = 3.0\text{ nC} + (4.7 - 4.8)\text{ nC} = 2.9\text{ nC}$$

$$Q_{SLEW\_F} = Q_{GD} \pm \Delta Q_{G(OD)} = 3.0\text{ nC} + (12.8 - 12.3)\text{ nC} = 3.5\text{ nC}$$

Since the value chosen for t_{SLEW} applies to both rising and falling slopes, the *larger* of the resulting Q_{SLEW_R} or Q_{SLEW_F} values (3.5 nC > 2.9 nC) drives the solution for an appropriate value I_{SRX} needed to satisfy the target t_{SLEW} time.

For this worked example, an assumed target slew time *t_{SLEW} = 1 µs* is targeted. Using the larger Q_{SLEW_F} computed value and rearranging equation 23 yields

$$I_{SRX} = \frac{Q_{SLEW\_F}}{t_{SLEW}} = \frac{3.5\text{ nC}}{1\ \mu\text{s}} = 3.5\text{ mA}$$

The pre−driver products' datasheets provide the available I_{SRX} slew current parameters together with a range of representative Q_{GD} values which are used to construct a slew time solution from those given in Table 3 below[5].

5. From the table it can be seen that if a unit charge value Q_{GD} = 1 nC is used together with a slew current value, the result is a unit slew time µs/nC that can be used to scale the slew time via the actual target Q_{GD} value.

Table 3. RISING/FALLING SLOPE SLEW SOLUTIONS

		Rising/Falling Slope Slew Current I_{SRX} (mA): SR_CTRL[2:0]							
		1.50	2.25	3.38	5.25	7.88	11.63	17.25	25.50
		Slew Time t_{SLEW} (μs)							
Target MOSFET Q_{GD} (nC)	1.00	0.67	0.44	0.30	0.19	0.13	0.09	0.06	0.04
	2.00	1.33	0.89	0.59	0.38	0.25	0.17	0.12	0.08
	3.00	2.00	1.33	0.89	0.57	0.38	0.26	0.17	0.12
	4.00	2.67	1.78	1.18	0.76	0.51	0.34	0.23	0.16
	5.00	3.33	2.22	1.48	0.95	0.63	0.43	0.29	0.20
	6.00	4.00	2.67	1.78	1.14	0.76	0.52	0.35	0.24
	7.00	4.67	3.11	2.07	1.33	0.89	0.60	0.41	0.27
	8.00	5.33	3.56	2.37	1.52	1.02	0.69	0.46	0.31
	9.00	6.00	4.00	2.66	1.71	1.14	0.77	0.52	0.35

Choosing $I_{SRX} = 3.38\ mA$ and substituting this value into equation 23 gives

$$t_{SLEW\_F} = \frac{Q_{SLEW\_F}}{I_{SRX}} = \frac{3.5\ nC}{3.38\ mA} = 1.04\ \mu s$$

Dynamic VDS Delay Time and Blanking Time Selection

Having determined a solution for t_{SLEW}, a dynamic VDS overload delay time can be selected from the values in Figure 7 below[6]. A value of $t_{DLYX} = 1.20\ \mu s$ is chosen for dynamic VDS delay, which satisfies the $t_{DLYX} > t_{SLEW}$ timing constraint of equation 12 (i.e. 1.20 μs > 1.04 μs) and provides a 15.4% margin:

$$\left(\frac{1.20\ \mu s}{1.04\ \mu s} - 1\right) \times 100\% = 15.4\%$$

Using the I_{PRCX} value chosen to construct the t_{SLEW} solution now allows a t_{BLANK} solution to be constructed via equation 14. Substituting the values for t_{PRCX} and Q_{SLEW_F}, and the target MOSFET's Q_{GS} value together with the chosen I_{SRX} solution yields:

$$t_{BLANK} > t_{PRCX} + \frac{(Q_{SLEW\_F} + Q_{GS})}{I_{SRX}}$$

$$t_{BLANK} > 200\ ns + \frac{(3.5 + 4.7)\ nC}{3.38\ mA} > 2.63\ \mu s$$

A blanking time $t_{BLANK} = 3.0\ \mu s$ is chosen from the pre−driver products' datasheets (Figure 7) which satisfies the timing constraint of equation 14 (i.e. 3.0 μs > 2.63 μs) and provides a 14.1% margin:

$$\left(\frac{3.0\ \mu s}{2.63\ \mu s} - 1\right) \times 100\% = 14.1\%$$

6. The T_DLYX[3:0] values in Figure 7 include the adjustment for tSYNC (50 ns typ.) as noted in the products' datasheet.

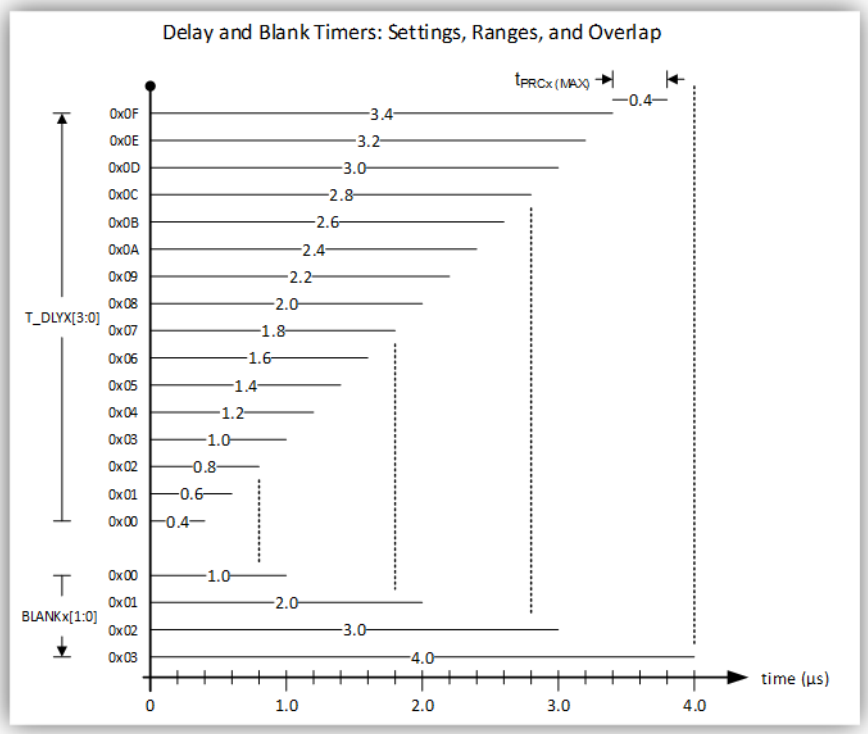

Figure 7. Dynamic VDS Detection Delay and Blanking Time Values – Datasheet Selections

Minimum 'ON' Time Solutions

The solutions for the high−side and low−side minimum 'ON' time intervals, defined respectively by equation 13 for the high−side (with t_{OD_R} expanded via equation 5 and t_{SLEW} replaced by t_{SLEW_R} and expanded via equation 23), and defined by equation 16 for the low side, can now be evaluated by substituting the values for the indicated parameters into those equations:

$$t_{ON(MIN\_HS)} = t_{BLANK} + t_{PRCX} + \frac{(Q_{SLEW\_R} + Q_{GD(OD)})}{I_{SRX}}$$

$$t_{ON(MIN\_HS)} = \left(3.0 + 0.2 + \frac{(2.9 + 12.8)\ nC}{3.38\ mA}\right)\ \mu s = 7.84\ \mu s \qquad \text{eq. 13}$$

$$t_{ON(MIN\_LS)} = 2 \times t_{BLANK} + t_{DLYX}$$

$$t_{ON(MIN\_LS)} = 2 \times 3\ \mu s + 1.2\ \mu s = 7.20\ \mu s \qquad \text{eq. 16}$$

Note the relative symmetry of the high−side and low−side minimum 'ON' time intervals.

PWM Deglitch Time

Two types of adaptive deglitch time t_{PWM_DGL} intervals are defined in the pre−driver products' datasheets, and they are re−stated here as t_{PWM_DGL1} and t_{PWM_DGL2} respectively for type 1 and type 2:

$$t_{PWM\_DGL1} = t_{BLANKX} + t_{PRCX} + t_{DLYX} \qquad \text{(eq. 26)}$$

$$t_{PWM\_DGL2} = t_{PRCX} + t_{DLYX} \qquad \text{(eq. 27)}$$

Evaluating these two equations by substituting the necessary parameters yields:

$$t_{PWM\_DGL1} = t_{BLANKX} + t_{PRCX} + t_{DLYX}$$

$$t_{PWM\_DGL1} = (3.0 + 0.2 + 1.2)\ \mu s = 4.40\ \mu s \qquad \text{eq. 26}$$

$$t_{PWM\_DGL2} = t_{PRCX} + t_{DLYX}$$

$$t_{PWM\_DGL2} = (0.2 + 1.2)\ \mu s = 1.40\ \mu s \qquad \text{eq. 27}$$

With either de−glitch type, a state change at the PWMx input must be maintained for at least as long as the t_{PWM_DGL} time in order for the change to be propagated to the gate pre−driver. Referring to Figure 4 it can be seen that the de−glitch is applied to both the rising and falling edges of the PWMx input signal and so applies a symmetrical time delay between the external and internal signals.

Evaluating the minimum 'ON' time values obtained via equation 13 and equation 16 vs. the boundary condition requirement of equation 17 by substituting the result obtained via equation 26 yields:

$$t_{ON(MIN\_HS)} > t_{PWM\_DGL1};\ 7.84\ \mu s > 4.40\ \mu s$$

$$t_{ON(MIN\_LS)} > t_{PWM\_DGL1};\ 7.20\ \mu s > 4.40\ \mu s \qquad \text{eq. 17}$$

Since $t_{DGL1} > t_{DGL2}$, the boundary condition requirement is satisfied for both the high−side and the low−side minimum 'ON' times using either de−glitch type.

PWM Duty Ratio Solutions

The duty ratio ‘D’ achievable with period T_{PWM} (or frequency f_{PWM}) is bounded by the minimum high−side and low−side ‘ON’ time values as defined via equation 18. Rearranging equation 18 gives solution forms for the bounded values of ‘D’:

$$D \geq f_{PWM(MAX)} \times t_{ON(MIN\_HS)} \quad \text{(eq. 28)}$$

$$D \leq 1 - (f_{PWM(MAX)} \times t_{ON(MIN\_LS)}) \quad \text{(eq. 29)}$$

Using the recommended $f_{PWM(MAX)}$ = 25 kHz value in the products’ datasheets and substituting the values computed for t_{DGL1} and respectively $t_{ON(MIN\_HS)}$ and $t_{ON(MIN\_LS)}$ into equation 28 and equation 29 gives

$$D \geq 25\ kHz \times 7.84\ \mu s \times 100\% \geq 19.6\% \quad \text{eq. 28}$$

$$D \leq 1 - (25\ kHz \times 7.20\ \mu s) \times 100\% \geq 82.0\% \quad \text{eq. 29}$$

For seat positioning applications, 23% duty may be low enough for minimum motor torque, but 79% might be too low for peak torque loads. Assuming a minimum $f_{PWM(MIN)}$ = 15 kHz value (which is typically the upper limit of human hearing) and substituting yields

$$D \geq 15\ kHz \times 7.84\ \mu s \times 100\% \geq 11.8\% \quad \text{eq. 28}$$

$$D \leq 1 - (15\ kHz \times 7.20\ \mu s) \times 100\% \leq 89.2\% \quad \text{eq. 29}$$

If power dissipation in the low−side MOSFET is not a concern, then passive recirculation may be allowed and the maximum achievable duty ratio may be extended via equation 20 so that

$$D_{(MAX)} \leq 1 - (f_{PWM} \times 2 \times t_{BLANK})$$

$$D_{(MAX)} \leq 1 - (15\ kHz \times 2 \times 3.0\ \mu s) \times 100\% \leq 91.0\% \quad \text{eq. 20}$$

Charge Pump Loading vs f_{PWM}

Finally, having determined the allowable PWM timing requirements, charge pump loading needs to be considered so that the charge pump’s capability is not exceeded. For example, evaluating $I_{CP(DC)}$ = 15 mA and f_{PWM} = 15 kHz and assuming zero static load I_{DC} gives

$$Q_{G(TOT\_SS)} = 2 \times \left(\frac{I_{CP(DC)} - I_{DC}}{f_{PWM}} \right) = 2 \times \left(\frac{(15 - 0)\ mA}{15\ kHz} \right)$$

$$Q_{G(TOT\_SS)} = 2000\ nC \quad \text{eq. 21}$$

This $Q_{G(TOT\_SS)}$ result is allocated, according to the respective MOSFETs’ gate charge requirements, among the number of channels in the application expected to concurrently operate in PWM mode.

Test Bench Load

As a final note, to properly model and observe the slope behavior of the high−side MOSFET – in particular the falling slope – on a test bench, an inductive test load needs to be used so that a ‘continuous’ load current (i.e. stable operating point) is provided. The load tau should to be on the order of 10x to 20x of the PWM period. The inductor’s ‘self−resistance’ can be dimensioned according to:

$$\frac{L_{LOAD} \times f_{PWM}}{20} \leq R_{LOAD} \leq \frac{L_{LOAD} \times f_{PWM}}{10} \quad \text{(eq. 30)}$$

Summary

The NCV7544, NCV7546, and NCV7547 N−MOSFET pre−drivers provide selectable charge and discharge currents that are used together with a MOSFETs’ gate charge parameters[7] to construct controlled switching slopes. The drive strategy can help minimize EMI and provides a means for faster overload response via dynamic overload detection[8]. The high−side drivers provide the selected drive currents in a phased sequence of pre−charge, slew, and overdrive intervals, while the low−side drivers provide drive current within a single interval.

The pre−charge interval is constructed using a fixed timer and a range of pre−charge currents to match a target MOSFET’s gate−source charge Q_{GS}. The slew interval is the time during which the high−side MOSFET’s gate−source voltage $V_{(GHx,\ HBx)}$ transitions through a ‘plateau’ region, where it’s gate and source are moving at the same rate. The desired slew time for both the rising and falling HBx switching is constructed using a range of slew currents and the MOSFET’s gate−drain charge Q_{GD}. The overdrive interval is constructed (or rather defined) by the same current as in the slew interval and the MOSFET’s total gate charge $Q_{G(TOT)}$ at V_{GS} = 10 V, minus the sum of the Q_{GS} and Q_{GD} charges.

A dynamic VDS overload detection delay time is used match the slew time to a range of selectable delay times so that the detection window opens at the expected point on the high−side or low−side MOSFET’s turn−on slope. In the case of the high−side, the delay time is started at the end of the pre−charge time. In the case of the low−side, the delay time is started concurrent with the drive current. The switching node voltage is compared with the appropriate overload detection threshold at the end of the delay time.

Ideally, the time needed for the high−side MOSFET to transition through the slew interval is the same for both the rising and falling slopes. However, while the same pre−charge time is applied to both slopes, the interval’s charge and discharge currents are selected based on how much gate charge must be added or removed to optimize the switching slope, and can cause variation between the rising and the falling slew time which may lead to dynamic overload ‘nuisance faults’. Due to the finite number of pre−charge solutions, the resulting undershoot or overshoot may cause an abrupt initial step in the turn−on or turn−off slope (pre−charge overshoot) or a shoot−through hazard between the high−side and low−side MOSFETs (pre−charge undershoot).

7. The MOSFET’s gate charge parameters vary as a function of its temperature, drain current I_D, and drain voltage V_{DS}.
8. Dynamic overload detection available only with the NCV7544 and NCV7546 products.

The products support concurrent PWM operation of multiple channels within a specific product's charge pump capability, and within the frequency and duty ratio limitations imposed by the various timing interval solutions as constructed for a particular target MOSFET. A symmetrical adaptive de−glitch timer embedded in each PWM input's signal path provides the benefits of reduced actuator random torque jitter and assured proper operation of the dynamic VDS overload protection function.

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