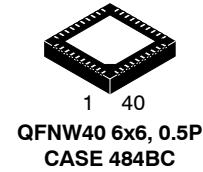


Bluetooth® 5.2 Wireless MCU

NCV-RSL15



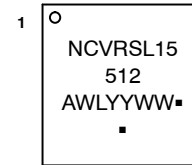
Introduction

RSL15 is an ultra-low power secure Arm® Cortex®-M33 processor-based Bluetooth Low Energy 5.2 wireless MCU designed for connected smart automotive applications. The comprehensive, yet easy-to-use Software Development Kit (SDK) provides sample applications that demonstrate the hardware capabilities to enable security with the Cybersecurity Platform, acquire sensor data in Smart Sense mode, configure the built-in power management and utilize Bluetooth Low Energy features. Specially designed and qualified for the unique needs of automotive, NCV-RSL15 comes in wettable flank-plated packaging, and a higher operating temperature range.

Key Features

- Automotive Ready
 - ◆ Wettable Flank-plated Packaging
- AEC-Q100 Grade 2
 - ◆ Operating Temperature Range -40°C to +105°C
 - ◆ PPAP Ready
- Bluetooth Low Energy 5.2 Certified with Key Features:
 - ◆ Up to 10 Simultaneous Connections
 - ◆ Long Range (Coded PHY)
 - ◆ 2 Mbit PHY (High Speed)
 - ◆ Angle of Arrival (AoA) and Angle of Departure (AoD)
 - ◆ Extended Advertising
 - ◆ Backwards Compatibility and Support for Earlier Bluetooth Low Energy Specifications Including 5.1, 5.0, 4.2, 4.1 and 4.0
- Ultra-low Power Operation:
 - ◆ Sleep Mode (GPIO Wakeup) @ 3 V VBAT: 40 nA
 - ◆ Sleep Mode (Crystal Oscillator, RTC Timer Wakeup) @ 3 V VBAT: 100 nA
 - ◆ Smart Sense Mode Allows Some Digital and Analog Peripherals to Remain Active to Monitor and Acquire Data from External Sensors at a Very Low System-level Power Consumption
 - ◆ Continuous ADC Operation in Smart Sense Mode with Wakeup on ADC Threshold @ 3 V VBAT: 206 nA
 - ◆ Peak Rx Current 1 Mbps @ 3 V VBAT: 2.7 mA
 - ◆ Peak Tx Current 0 dBm Output Power @ 3 V VBAT: 4.3 mA
 - ◆ Non-Connectable Advertising at 5 s Intervals @ 3 V VBAT: 1.1 µA (Average)
 - ◆ Connectable Advertising at 5 s Intervals @ 3 V VBAT: 1.3 µA (Average)
- Rx Sensitivity (BLE Mode, 1 Mbps): -96 dBm
- Rx Sensitivity (BLE Mode, 2 Mbps): -94 dBm
- Configurable Tx Power: -17 dBm to +6 dBm

MARKING DIAGRAM



NCVRSL15512 = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Throughout this document, in reference to memory sizes, the unit kB denotes 1024 Bytes.

Key Features (continued)

- Arm Cortex-M33 Processor Clocked up to 48 MHz
- Cybersecurity Platform with Arm CryptoCell™ -312 for End-to-end Product Security with Secure Boot, Root of Trust, Lifecycle Management, Secure Key Management, and Application and Data Security
- Arm TrustZone® to Enable Secure Execution Zones
- 512 kB Flash Memory
- 80 kB RAM (64 kB User RAM, 16 kB RAM for Baseband)
- Flexible Power Management: 1.2 V – 3.6 V VBAT. Directly Connect 1.5 V Silver-oxide or 3 V Coin Cells without Any External Active Components
- Two SPI Ports with QSPI Capability

NCV-RSL15

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------------------|------------------|----------------|
| NCV-RSL15-512-101Q40-AVG | QFNW40 (Pb-Free) | 3500 Tape/Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

APPLICATIONS

Automotive

- Smart Vehicle Access
- Tire Pressure Monitoring System (TPMS)
- Tire Monitoring System (TMS)
- Seat Belt Detection
- Cable Replacement
- Instrument Cluster

HIGH-LEVEL BLOCK DIAGRAM

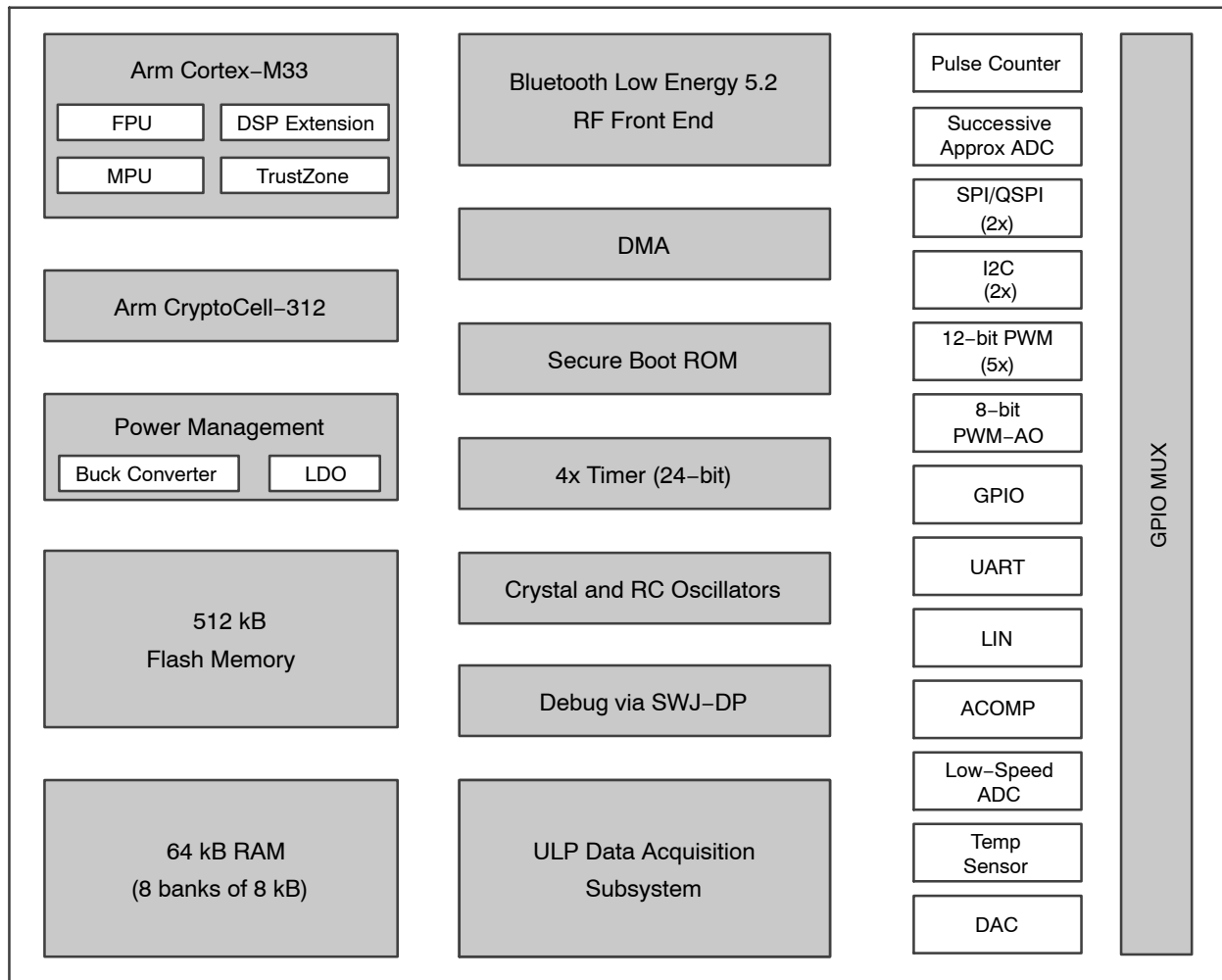


Figure 1. NCV High-Level Block Diagram

FEATURES

Arm Cortex-M33 Processor

The Cortex-M33 32-bit Armv8-M processor is designed for IoT and deeply embedded applications that require high performance, power efficiency and security. The processor has many features to execute high performance applications such as Floating-Point Unit (FPU), DSP extensions and Memory Protection Unit (MPU). Secure debug is done through the SWJ-DP which combines JTAG-DP and SW-DP for either JTAG probe or Serial Wire Debug (SWD) connection.

Cybersecurity Platform

The Cortex-M33 processor with TrustZone Armv8-M security extensions forms the basis of the security platform. The Arm CryptoCell-312 allows for end-to-end product security with Secure Boot with Root of Trust, secure lifecycle management, secure key management, and application and data encryption using symmetric or asymmetric cryptography. Arm TrustZone enables secure software access control. User available cryptographic services such as SHA1, SHA256, keyed-hash message authentication code (HMAC) and True Random Number Generator (TRNG) allow for development of custom proprietary security solutions. The TRNG conforms to NIST SP800-90B, NIST SP800-22, FIPS 140-2, and BSI AIS-31.

Please note that this mobile telecommunications Radio Access Network (RAN) equipment is designed for civil use, which also meet the provisions of paragraphs a.2 to a.4 of the Cryptography Note (Note 3 in Category 5—Part 2), having an RF output power limited to 0.1 W (20 dBm) or less, and supporting 16 or fewer concurrent users.

RF Subsystem

The RF architecture is based on a 2.4 GHz RF Front End that implements the physical layer of the BLE 5.2 standard as well as other proprietary or custom protocols. The modem is of the FSK type with a single-ended RF Port, which alleviates the need for an external balun.

RF Operation

Bluetooth 5.2 certified baseband and protocol stack has features such as 2 Mbps RF link, Angle-Of-Arrival, Angle-Of-Departure, and Coded PHY (“Long Range”). The hardware enables implementation of custom protocols.

Localization

RSL15 supports Angle-of-Arrival (AoA) and Angle-of-Departure (AoD) as defined by the Bluetooth Low Energy standard along with RSSI for enhanced localization capabilities.

Flexible Power Management

Built-in DC-DC converter with buck and LDO modes requiring few external passive components allows for a

broad voltage supply range. Any voltage in the range of 1.2 V to 3.6 V can be used directly without the need for external power conversion allowing for simple use of common coin cell batteries such as 3 V coins cells and 1.5 V silver oxide cells.

Power Modes

Several power modes are available to reduce power consumption while still maintaining system responsiveness. Each mode is configurable with RAM retention and wakeup sources. Smart Sense mode allows some digital and analog peripherals to remain active to monitor and acquire data from external sensors at a very low system-level power consumption.

Flexible Clocking

Two crystal oscillators and two internal RC oscillators are available on RSL15 to offer many clocking configurations. The primary oscillator is based on a 48 MHz crystal, which is necessary for any connected RF operation. The secondary oscillator is based on a 32 kHz crystal, which can be used for precision timing even in low power modes. When precision timing is not required, the internal fast RC oscillator can be used in place of the 48 MHz crystal oscillator for general non-RF processing. Likewise, the internal 32 kHz RC oscillator can be used in place of the 32 kHz crystal oscillator for certain use cases. Additionally, 48 MHz and 32 kHz external clocks can be driven into RSL15 from external clock sources.

Analog to Digital Converters (ADCs)

RSL15 has two ADCs, a high-speed 12-bit SAR ADC for fast conversion of analog inputs up to 2 Msps and Low Speed ADC for slower conversion up to 50 ksps. There is also an integrated temperature sensor that can be read by the Low Speed ADC.

Flexible I/O

General purpose I/O can be mapped to GPIO, SPI, QSPI, I2C, UART, LIN, PWM, PCM, pulse counter, clock input/output and analog functions. RSL15 facilitates an analog comparator, as well as a DAC for generating bias voltages for external components.

Memory Architecture

The memory architecture is centered around the Arm Cortex-M33. The flash memory contains application code as well as the protocol stack. The RAM architecture is flexible allowing for powering only the amount of memory needed for the application. A total of 64 kB user RAM is available, implemented as eight times 8 kB. An additional 16 kB is available for the digital baseband hardware. A DMA controller is available for easy data streaming between a peripheral/interface and memories.

NCV-RSL15

Software Development Kit

Contains Eclipse-based **onsemi** IDE plus support for other industry standard development environments, Bluetooth protocol stack, sample applications, libraries and many other software components and tools to enable rapid application development.

RoHS Compliant Device

RSL15 is RoHS compliant.

ARCHITECTURE OVERVIEW

Introduction

RSL15 is a highly integrated secure Arm Cortex-M33 based Bluetooth Low Energy 5.2 wireless MCU system-on-chip with flash and RAM, built-in power

management and an extensive set of peripherals. The wide supply voltage input, flexible I/O and clocking scheme offer maximum design flexibility.

Detailed Block Diagram

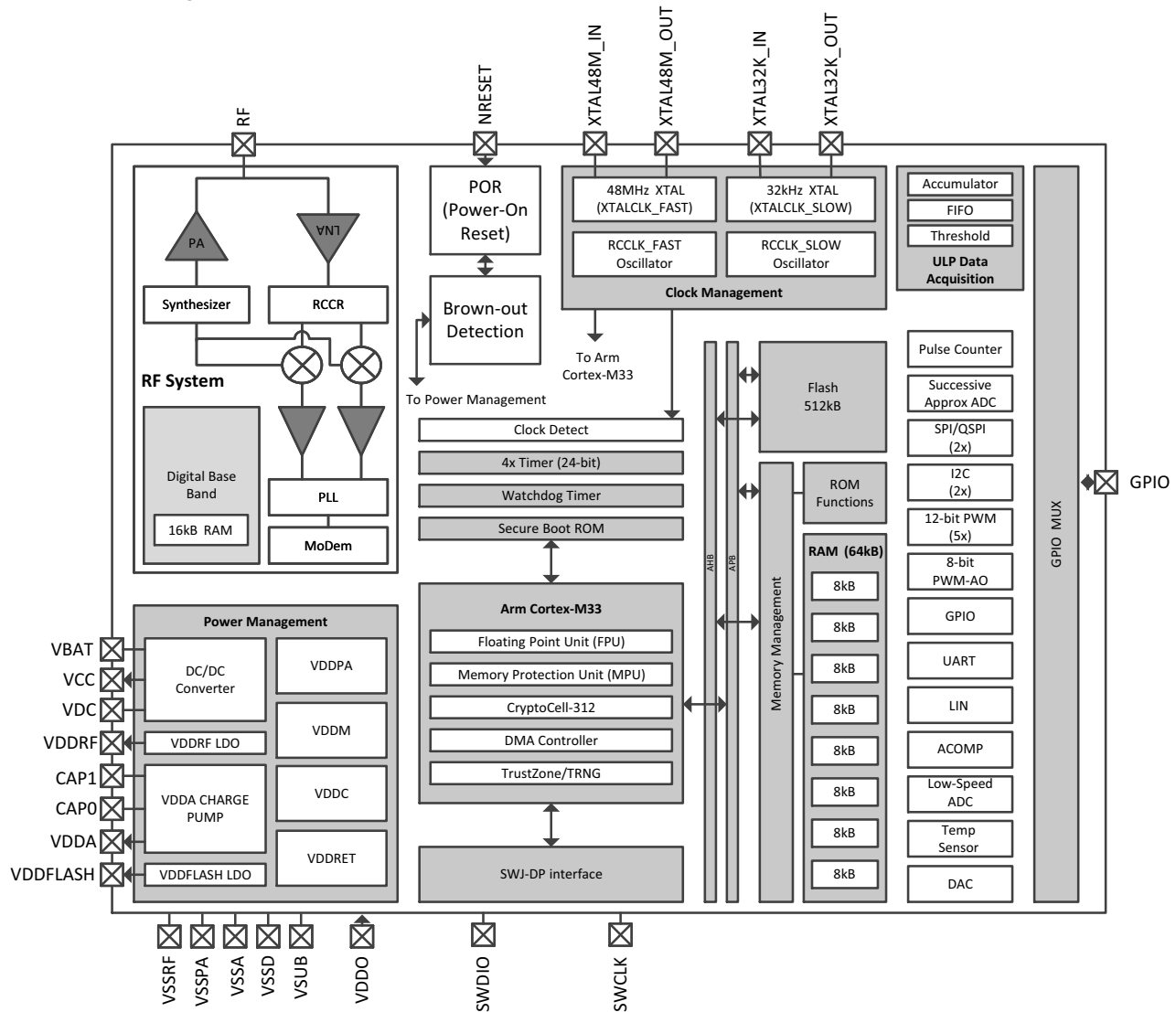


Figure 2. NCV-RSL15 Detailed Block Diagram

Arm Cortex-M33 Processor

The Cortex-M33 32-bit Armv8-M processor is designed for IoT and deeply embedded applications that require high performance, power efficiency and security. The processor has many features to execute high performance applications such as Floating-Point Unit (FPU), DSP extensions and Memory Protection Unit (MPU). Secure debug is done through the dedicated Serial Wire Debug Port (SW-DP) interface.

DMA Controller

The Direct Memory Access (DMA) Controller allows background transfers between peripherals and memories without processor intervention. The processor can be in a low power state or used for other computational tasks while the transfer occurs. The DMA is connected to the processor, peripherals and RAM memories and has four independent channels.

Cybersecurity Platform

The Cortex-M33 processor with TrustZone Armv8-M security extensions forms the basis of the security platform that is extended with Arm CryptoCell-312.

Secure Boot with Root of Trust

The secure boot ROM authenticates firmware in flash with a certificate-based mechanism using a private-public key scheme. This is the basis of the hardware Root of Trust. This same mechanism ensures continuity of the hardware Root of Trust after secure Firmware-Over-The-Air (FOTA) update.

Data and Application Encryption

User available cryptographic services including AES-128, AES-256, SHA-256, Hash Message Authentication Code (HMAC), PKA (Public Key Accelerator), ChaCha and AIS-31 compliant True Random Number Generator (TRNG) allow for development of custom proprietary security solutions.

TrustZone

Enables secure software access control to protect critical software and hardware resources.

Secure Lifecycle State Management

Lifecycle states refers to the multiple states RSL15 could go through during its lifetime. The first lifecycle state is the Chip Manufacture (CM) Lifecycle State. The device manufacture transitions to the Device Manufacture (DM) Lifecycle State. At field deployment, it is transitioned to the Secure (SE) Lifecycle State. A Return to Manufacturer (RMA) State is also available. Lifecycle state management ensures the authenticity, integrity and confidentiality of code and data belonging to different stakeholders at each lifecycle.

In addition to the Secure Lifecycle States, an Energy Harvesting (EH) Mode is available for applications that require fast cold startup (initial application of VBAT) but do not require secure boot with Root of Trust. This mode is

especially useful when RSL15 is used in energy harvesting systems.

RF Subsystem

The RSL15 2.4 GHz radio front-end implements the physical layer for the Bluetooth Low Energy standard and other standard, proprietary, or custom protocols.

It operates in the worldwide deployable 2.4 GHz ISM band (2.4000 to 2.4835 GHz).

RF Architecture

The 2.4 GHz radio front-end is based on a low-IF architecture and comprises the following building blocks:

- High performance single-ended RF port which alleviates the need for an external balun
- On-chip matching network with 50 Ω RF input
- Low power LNA (low noise amplifier), and mixer
- PA (Power Amplifier) with up to +6 dBm output power for Bluetooth
- RSSI (Received Signal Strength Indication) with 60 dB nominal range with 1 dB steps (not considering AGC)
- Fully integrated ultra-low power frequency synthesis with fast settling time, with direct digital modulation in transmission (pulse shape programmable)
- 48 MHz XTAL reference
- Fully-integrated FSK-based modem with programmable pulse shape, data rate, and modulation index
- Digital baseband (DBB) with link layer functionalities, including automatic packet handling with preamble & sync, CRC, and separate Rx and Tx 128-bytes FIFOs
- The 2.4 GHz radio front-end contains also a highly-flexible digital baseband – in terms of modulation schemes, configurability and programmability – in order to support Bluetooth Low Energy technology and proprietary protocols. It allows for programmable data rates from 62.5 kbps up to 2 Mbps, FSK with programmable pulse shape and modulation index.
- The 2.4 GHz radio front-end also includes Manchester encoding and Data whitening. The packet handling includes:
 - ◆ Automatic preamble and sync word insertion
 - ◆ Automatic packet length handler
 - ◆ Basic address check
 - ◆ Automatic CRC calculation and verification with a programmable CRC polynomial
 - ◆ Multi-frame support
- Coexistence signals to identify the RF front-end is busy for Bluetooth or other traffic

Bluetooth Low Energy

RSL15 is Bluetooth 5.2 certified with the following Bluetooth LE features:

- Angle of Arrival (AoA) and Angle of Departure (AoD)
- LE Long Range (Coded PHY)

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- 2 Mbit PHY (High Speed)
- LE Extended Advertising
- High Duty Cycle Non-Connectable Advertising
- LE Channel Selection Algorithm #2
- Advertising Channel Index
- GATT Caching
- HCI support for debug keys in LE Secure Connections
- Sleep clock accuracy update mechanism
- ADI field in scan response data
- Host channel classification for secondary advertising
- Periodic Advertising Sync Transfer

- Backwards compatibility and support for earlier Bluetooth Low Energy specifications including 5.1, 5.0, 4.2, 4.1 and 4.0

Power Management

The flexible power management of RSL15 allows for a wide range of battery voltages without the need for external power conversion. Two key modes of the DC-DC converter are:

1. BUCK Mode Operation
2. LDO Mode Operation

The power management unit is shown in Figure 3.

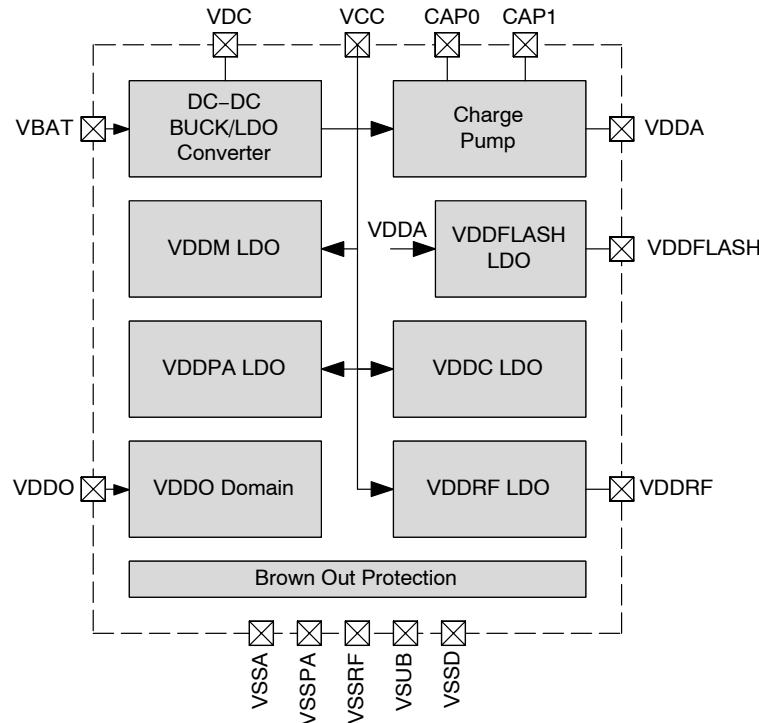


Figure 3. Power Management Unit

BUCK Mode can be used for battery voltages above 1.4 V. In this case the internal DC-DC converter regulates the battery voltage VBAT to a voltage VCC of approximately 1.2 V. The VCC voltage is then converted (using a charge pump) to an approximate 2.4 V voltage VDDA, which is used to power the analog blocks (excluding the RF Blocks). VCC and VDDA require external capacitors. Additionally, BUCK Mode Operation requires an inductor to be placed between the VCC and VDC pins.

LDO Mode is typically used for battery voltages at 1.4 V and below (but can be used for the entire operating voltage). In this case a linear LDO generates a voltage VCC of 1.2 V. A charge pump then generates a 2.4 V voltage for the analog blocks.

VDDRF is a regulated voltage used to supply the RF system. VDDRF is trimmed by **onsemi** as part of the device manufacturing process.

A separate supply exists for powering the flash, i.e. VDDFLASH. VDDFLASH is trimmed by **onsemi** as part of the device manufacturing process.

Three additional regulators generate voltages for the system (none require external components):

- VDDC is the voltage for the internal digital blocks – excluding digital RAM and GPIOs. VDDC is trimmed by **onsemi** as part of the device manufacturing process
- VDDM is the voltage for the RAM blocks. VDDM is trimmed by **onsemi** as part of the device manufacturing process
- VDDPA is the voltage used to supply the RF power amplifier (used in RF Tx mode). The VDDPA setting depends on the output power level selected

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VDDO is an input to the RSL15 and constitutes the logical high level for the digital I/Os, i.e. if VDDO is connected to VBAT the GPIO signal swing will be between GND and VBAT.

The RSL15 power management unit allows for operation across wide temperature and voltages ranges at low power consumption and monitors the battery voltage to ensure reliable operation. If the battery voltage dips below the Power-On Reset (POR) voltage, a POR is asserted to the system. This also prevents possible damage to RSL15 when the battery is inserted or removed.

Reset

The Power Management Unit automatically resets the internal systems during power supply disruptions such as insufficient battery voltage or during battery insertion/removal. Upon power supply rise (such as battery insertion), the system is held in Power-On-Reset until sufficient internal voltages are reached and stabilized. When POR is released, the boot ROM execution begins using the RCCLK clock @ 3 MHz.

A reset can also be issued by software, watchdog timer expiration, invalid or missing clock detected by the clock detector, or by asserting the nRESET pin.

Power Modes Overview

The power modes are available to reduce power consumption while still maintaining system responsiveness.

The low power modes are Sleep, Standby, Smart Sense and Idle.

Sleep Mode is the lowest power mode but with the longest wakeup time.

Standby Mode is low power but with faster wakeup time than Sleep Mode.

Smart Sense mode takes advantage of the low power capability of Sleep Mode but also allows some digital and analog peripherals to remain active with minimal processor intervention. Smart Sense mode allows RSL15 to not only remain responsive to external events, but also monitor and acquire data from external sensors with very low system-level power consumption.

Idle Mode allows for some power savings with the fastest wakeup time through disabling of internal clocks.

Sleep, Standby and Smart Sense modes have the ability of RAM retention (configurable amount of RAM to be retained) and allow for configurable wakeup sources.

Wakeup sources include GPIO transition (pin-based wakeup), timer, comparator, ADC threshold or sample FIFO full.

An overview of the power modes is shown in Table 1. The peripherals and subsystems available in each power mode are described below.

Table 1. POWER MODES OVERVIEW

| Power Mode | Description |
|------------------|--|
| Sleep Mode | The lowest power mode. Processor and RF subsystem powered down and not clocked. Only selected wakeup sources are powered. Memory retention (and amount of memory retained) is optional. Some peripherals are available in Sleep Mode. On wakeup, the ROM restores the system before program execution begins. |
| Smart Sense Mode | Smart Sense Mode takes advantage of the low power capability of Sleep Mode but also allows some digital and analog peripherals to remain active with minimal processor intervention. Smart Sense Mode allows RSL15 to not only remain responsive to external events, but also monitor and acquire data from external sensors at a very low system-level power consumption. |
| Standby Mode | A low power mode with faster wakeup time than Sleep Mode. Processor and RF subsystem powered with lower voltage and not clocked. Only selected wakeup sources are powered. Memory retention (and amount of memory retained) is configurable. Some peripherals are available in Standby Mode. On wakeup, the program is executed directly out of retained RAM. |
| Idle Mode | A mode to save power for a short period of time when very fast wakeup is required. Processor, RF subsystem and memory powered as in Run Mode but not clocked. |
| Run Mode | Processor, RF subsystem and memory powered normally – clocks are active, all peripherals available. |

Peripherals and Subsystems Availability in Power Modes

The different power modes allow for low power operation in many types of applications. When applications utilize one or more external sensors that require continued biasing regardless of the power mode of RSL15, it may be possible to use the VDDA voltage for this purpose.

VDDA can be kept active even in Sleep, Smart Sense and Standby Modes.

Table 2 describes the peripherals available in all power modes.

Table 2. POWER MODE PERIPHERAL AVAILABILITY

| Component | Power Mode | | | | |
|--------------------------------|------------|------|-----------|-------------|-----------|
| | Run | Idle | Standby | Smart Sense | Sleep |
| Processor | On | On | Off | Off | Off |
| Baseband/RF | On | On | Off | Off | Off |
| RAM Retention | N/A | N/A | N/A | Available | Available |
| CryptoCell | On | On | On or Off | On or Off | On or Off |
| RTC | On | On | On or Off | On or Off | On or Off |
| ULP Data Acquisition Subsystem | On | On | On or Off | On or Off | Off |
| Successive Approximation ADC | On | On | On or Off | On or Off | Off |
| Pulse Counter | On | On | On or Off | On or Off | Off |
| Comparator | On | On | On or Off | On or Off | On or Off |
| DAC | On | On | Off | Off | Off |
| ACS-PWM | On | On | On or Off | On or Off | On or Off |
| PWM | On | On | Off | Off | Off |
| Low Speed ADC | On | On | Off | Off | Off |
| 32k Clock Output | On | On | On or Off | On or Off | On or Off |
| I2C | On | On | Off | Off | Off |
| SPI | On | On | Off | Off | Off |
| UART | On | On | Off | Off | Off |
| LIN | On | On | Off | Off | Off |
| PCM | On | On | Off | Off | Off |
| Temp Sensor | On | On | Off | Off | Off |

ULP Data Acquisition Subsystem

The ULP Data Acquisition Subsystem comprises a small FIFO, Accumulator and Threshold Comparator that can be used in combination with the Successive Approximation ADC and pulse counter to perform data acquisition and rudimentary data processing and decision making. Available in all power modes.

This enables simple processing and storage of a limited number of samples from a pulse counter or the Successive Approximation ADC while in the low power mode, Smart Sense mode, for the lowest power operation.

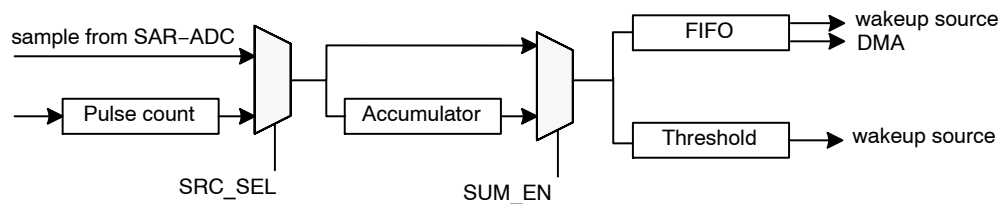


Figure 4. ULP Data Acquisition Subsystem.

The ULP Data Acquisition Subsystem has various features to further reduce power consumption such as Burst Sampling Mode, which allows for bursts of high speed sampling followed by an adjustable delay between sampling bursts.

The pulse counter can be configured to accept inputs from any of GPIO[3:0]. It counts pulses from these GPIOs during a set window ranging from 1 to 1024 clock cycles (based on a 32 kHz clock).

Overall, the ULP Data Acquisition Subsystem operation can be summarized as follows:

Accumulation

- An accumulation can be done with a configured number of samples ranging from 1 to 16 samples
- This mode is enabled when SUM_EN is set on Figure 4
- The accumulated value is stored in the FIFO

Threshold Detection

- Two thresholds can be configured: one when the input value goes higher than the threshold, and one when the input value goes lower than the threshold
- This mode allows the system to wake up after a configured number of consecutive samples generated are greater than or lower than the configurable threshold.

Acquisition

- Acquired samples are stored in the FIFO. FIFO size can be 1 to 16 samples

Clocking

Oscillators

The following oscillators are available:

- 48 MHz crystal oscillator (RFCLK) typically used in RUN Mode when RF operation is required. Prescalers exist to provide divided clocks (including system clock) to other parts of the system
- A fast RC oscillator (RCCLK) can provide an alternative to the 48 MHz crystal oscillator. However, RF operation is not possible using the fast RC Oscillator
- A 32 kHz crystal oscillator (XTAL32K) typically used in Sleep and Standby Modes for precision timing and to maintain the real-time clock (RTC)
- A slow RC oscillator (RC32) that can be an alternative to the 32 kHz crystal oscillator for certain use cases.

Clock Management

Flexible clock management allows the different clock sources to be used in power-efficient ways and to minimize

external components. Internal RC oscillators can be used for fast startup and then easily switched to crystal oscillators when precision timing is required. Additionally, clocks can be sourced externally with the 48 MHz and 32 kHz clock inputs.

A built-in clock detector ensures a proper system reset in case the system clock goes below 2 kHz.

General Purpose Input/Output (GPIO)

RSL15 contains highly flexible general purpose input/output (GPIO) pins that can be configured as digital input or output, communication interfaces, clocks, wakeup sources or analog functions. Communication interfaces can be routed to any GPIO. Other functions are available on select GPIO, see section Pin Definition and Multiplexing.

Each GPIO has a software configurable pull up/down resistor, debounce LPF for I2C and four drive strengths options.

Analog

Successive Approximation ADC (SAR ADC)

The Successive Approximation ADC (SAR ADC) generates 12-bit samples up to 2 Msps sample frequency.

The SAR ADC is auto calibrated during operation for optimal INL/DNL performance.

Low Speed ADC Converter (LSAD)

This is a combined integrating and algorithmic ADC that has a resolution varying from 8 to 14 bits depending on configuration. While converting, the input signal can be integrated across one or more clock cycles (depending on configuration). ADC sampling rate can be up to 50 ksp/s. This ADC converter is also used to monitor the VBAT input voltage. It can also be configured to measure single ended or differential input voltages.

Pulse Counter

A pulse counter can be driven by one of GPIO[3:0]. It counts pulses from these GPIOs during a set interval.

Analog Comparator

RSL15 contains a low-power comparator that can be active in Standby, Sleep and Smart Sense mode. It has 3 different settings to trade off response time with power consumption, Low Power, Normal and High Speed, see section Analog Comparator Specifications (ACOMP).

DAC

RSL15 contains a low-power DAC that can be used for sensor biasing purposes. To optimize power consumption there is also a buffer that can be disabled if the load is high impedance.

Peripherals

Timers

There are four independent 24-bit timers that can operate as single-shot, multi-shot or free-run. An interrupt can be generated on timer expiration. Also, a GPIO interrupt can capture and store the current timer value.

Watchdog

The independent watchdog timer cannot be disabled. It must be reloaded at regular intervals. At the first timer expiration, an interrupt is generated and the timer is reloaded. At the second timer expiration, a reset is issued to the system.

PWM

The PWM (Pulse Width Modulation) controller can output on five independent channels with configurable period, duty cycle and offset. The PWM has 12-bit resolution with an optional 8-bit dithering per channel for lighting applications.

Additionally, one 8-bit ACS-PWM channel fixed on GPIO[4] can be operational in low power modes.

I2C

The I2C controller consists of 2 independent channels of the two-wire interface including a bidirectional clock line (SCL) and bidirectional data line (SDA). The I2C interface supports both master and slave mode operation. 100 kHz, 400 kHz and 1 MHz modes are supported.

SPI

The SPI controller consists of 2 independent channels with the standard 4-wire interface of SCLK, MOSI, MISO and CS supporting master and slave mode. Each channel also supports dual (DSPI) and quad (QSPI) modes in half or full duplex mode.

UART

The general-purpose Universal Asynchronous Receiver-Transmitter (UART) uses a standard data format with one start bit, eight data bits and one stop bit.

LIN

The Local Interconnect Network (LIN) is an asynchronous 2-wire interface. The LIN module operates as a responder node on the bus, supporting version 2.2 of the LIN specification.

PCM

The highly configurable PCM (Pulse Code Modulation) interface can be used to stream data in and out of RSL15.

RTC

The RTC timer consists of a 32-bit free-running up-counter, clocked by the 32 kHz clock.

Activity Counter

The activity counters help to analyze how long the system has been running, and how much the CPU and the flash have been used by the application in a period of time. This is useful information to estimate and optimize the power consumption of the application.

Asynchronous Clock Counter

The asynchronous clock counter measure the timing of a clock signal, such as STANDBYCLK or a clock provided on a GPIO input, relative to the system clock.

CRC

This block provides an implementation of two standard cyclic redundancy code (CRC) algorithms (CRC-CCITT and CRC-32) which, if used, can ensure data integrity of a user application's code and data.

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Memory Map

The RSL15 memory map is shown in Figure 5 (512 kB flash version only).

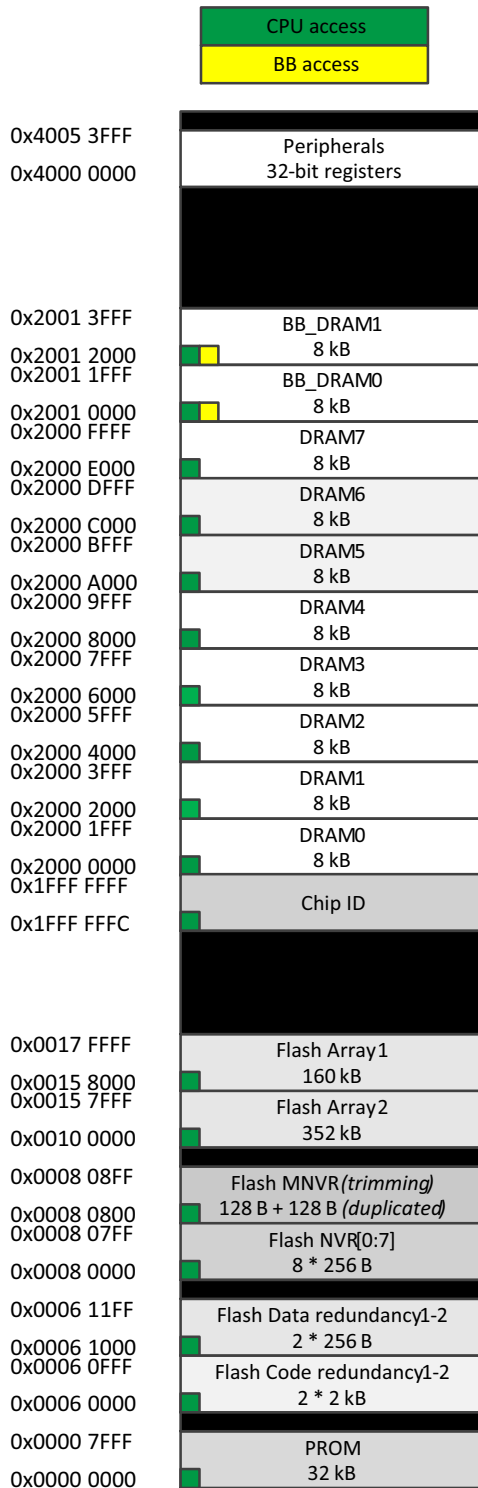


Figure 5. RSL15 Memory Map

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 3. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|-------------------------|--|------------|------------|------|
| VBAT | Power supply voltage input | | 3.63 | V |
| VDDO | Digital I/O supply voltage input | | 3.63 | V |
| VSSRF | RF front-end ground | -0.3 | | V |
| VSSA | Analog ground | -0.3 | | V |
| VSSC | Digital ground | -0.3 | | V |
| V _{in} | Voltage at any input pin | VSSC - 0.3 | VDDO + 0.3 | V |
| V _{in} to LSAD | Voltage at GPIO selected as LSAD input | VSSA - 0.3 | VDDA + 0.3 | V |
| RF | Maximum RF Input Power | | 18 | dBm |
| T _{stg} | Storage temperature range (Note 1) | -40 | 150 | °C |
| T _J | Junction Temperature | | 125 | °C |

Stresses exceeding those listed in the Absolute Maximum Ratings table may damage the device.

CAUTION: Class 2 ESD Sensitivity, AEC-Q100-002 (JS-001) HBM ±2000 V on all pins.
 Class C1 ESD Sensitivity, AEC-Q100-011 (JS-002) CDM ±250 V on all pins.
 Class II level A Latch up immunity AEC-Q100-004 (JESD78) ±100 mA on all pins.

1. Storage temperature applies after soldering to PCB.

General Operating Conditions

Table 4. GENERAL OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|---|---|------------|------|------|------|
| VBAT | DC-DC Converter Input Voltage | BUCK Mode | 1.4 | | 3.6 | V |
| | | LDO Mode | 1.2 | | 3.6 | |
| | VBAT Supply Rise Time | Maximum rate of voltage rise | | | 0.1 | V/μs |
| VCC | DC-DC Converter / LDO Output Voltage (Note 2) | | 1 | 1.2 | 1.32 | V |
| VDDA | Analog Blocks Supply Voltage Output (Note 2) | VDDA is generated by a charge pump that doubles the VCC voltage | | 2.4 | | V |
| VDDFLASH | Flash Supply Voltage Output (Note 2) | | 0.75 | 1.75 | 2.3 | V |
| VDDO | Digital I/O Supply Input (Note 2) | | 1.2 | | 3.6 | V |
| VDDRF | RF Supply Output (Note 2) | | 1.0 | 1.1 | 1.21 | V |
| SYS_CLK | System Clock | | 8 (Note 3) | | 48 | MHz |
| | Operating Temperature | | -40 | | 105 | °C |
| VBAT _{POR} | POR Voltage | | 0.4 | 0.8 | 1.0 | V |

If any limits in the General Operating Conditions table are exceeded, device functionality should not be assumed. Exposure beyond maximum operating conditions for extended periods may affect device reliability.

2. VCC, VDDA, VDDFLASH and VDDRF Outputs are for connections to external filtering capacitors only. These regulated voltages are used internally and are not intended for powering external devices.
3. Minimum SYS_CLK required for BLE Operation.

System Clock

The following table lists the sources and valid frequencies of System Clock.

Table 5. SYSTEM CLOCK

| System Clock Frequency (MHz) | Source |
|------------------------------|------------------|
| 1 | EXTCLK |
| 3 | RC, EXTCLK |
| 8 | XTAL, EXTCLK |
| 12 | XTAL, RC, EXTCLK |
| 16 | XTAL, EXTCLK |
| 24 | XTAL, RC, EXTCLK |
| 32 | EXTCLK |
| 48 | XTAL, EXTCLK |

4. To write to flash, System Clock source must be XTAL. To operate BLE, System Clock source must be XTAL at 8MHz or higher.
5. EXTCLK is an external digital clock source.

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Power Consumption

RF Current Consumption

Table 6 shows key peak current consumption values for RF activity. Unless otherwise noted, the specifications

mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) active, Radio ON and internal supplies trimmed to factory defaults.

Table 6. RF CURRENT CONSUMPTION

| Operating Conditions | VBAT | DC Conversion | Min | Typ | Max | Unit |
|---|--------|---------------|-----|------|-----|------|
| Radio Receive Mode Rx @ 125 kbps, 2.4 GHz 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 2.9 | | mA |
| | 1.8 V | BUCK Mode | | 4.4 | | |
| | 1.25 V | LDO Mode | | 6 | | |
| Radio Receive Mode Rx @ 500 kbps, 2.4 GHz 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 2.9 | | mA |
| | 1.8 V | BUCK Mode | | 4.4 | | |
| | 1.25 V | LDO Mode | | 6 | | |
| Radio Receive Mode Rx @ 1 Mbps, 2.4 GHz 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 2.7 | | mA |
| | 1.8 V | BUCK Mode | | 4.3 | | |
| | 1.25 V | LDO Mode | | 5.8 | | |
| Radio Receive Mode Rx @ 2 Mbps, 2.4 GHz 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 3.2 | | mA |
| | 1.8 V | BUCK Mode | | 4.9 | | |
| | 1.25 V | LDO Mode | | 6.7 | | |
| Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 0 dBm 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 4.3 | | mA |
| | 1.8 V | BUCK Mode | | 6.7 | | |
| | 1.25 V | LDO Mode | | 9.1 | | |
| Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 3 dBm 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 8 | | mA |
| | 1.8 V | BUCK Mode | | 12.3 | | |
| | 1.25 V | LDO Mode | | 16.9 | | |
| Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 5 dBm 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 10.6 | | mA |
| | 1.8 V | BUCK Mode | | 16.5 | | |
| | 1.25 V | LDO Mode | | 22.5 | | |
| Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 6 dBm 8 MHz system clock Cortex-M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 11.4 | | mA |
| | 1.8 V | BUCK Mode | | 17.8 | | |
| | 1.25 V | LDO Mode | | 24.1 | | |

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Run Mode Current Consumption

Table 7 shows key current consumption values for Run Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck

mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) active, Radio OFF and internal supplies trimmed to factory defaults.

Table 7. RUN MODE CURRENT CONSUMPTION

| Operating Conditions | VBAT | DC Conversion | Min | Typ | Max | Unit |
|---|--------|---------------|-----|-----|-----|--------|
| 8 MHz system clock Executing CoreMark from Flash All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 49 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 76 | | |
| | 1.25 V | LDO Mode | | 106 | | |
| 16 MHz system clock Executing CoreMark from Flash All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 39 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 58 | | |
| | 1.25 V | LDO Mode | | 84 | | |
| 24 MHz system clock Executing CoreMark from Flash All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 34 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 54 | | |
| | 1.25 V | LDO Mode | | 77 | | |
| 48 MHz system clock Executing CoreMark from Flash All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 30 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 46 | | |
| | 1.25 V | LDO Mode | | 65 | | |
| 8 MHz system clock Executing CoreMark from RAM All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 33 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 50 | | |
| | 1.25 V | LDO Mode | | 71 | | |
| 16 MHz system clock Executing CoreMark from RAM All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 26 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 39 | | |
| | 1.25 V | LDO Mode | | 55 | | |
| 24 MHz system clock Executing CoreMark from RAM All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 20 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 31 | | |
| | 1.25 V | LDO Mode | | 51 | | |
| 48 MHz system clock Executing CoreMark from RAM All peripherals disabled 64 kB RAM enabled | 3.0 V | BUCK Mode | | 21 | | μA/MHz |
| | 1.8 V | BUCK Mode | | 34 | | |
| | 1.25 V | LDO Mode | | 50 | | |

Idle Mode Current Consumption

Table 8 shows key current consumption values for Idle Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck

mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) active, Radio OFF and internal supplies trimmed to factory defaults.

Table 8. IDLE MODE CURRENT CONSUMPTION

| Operating Conditions | Wakeup Source | VBAT | DC Conversion | Min | Typ | Max | Unit |
|---|---------------|--------|---------------|-----|-----|-----|------|
| System clock stopped 64 kB RAM enabled | GPIO | 3.0 V | BUCK Mode | | 128 | | μA |
| | | 1.8 V | BUCK Mode | | 103 | | |
| | | 1.25 V | LDO Mode | | 156 | | |

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Standby Mode Current Consumption

Table 9 shows key current consumption values for Standby Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT =

VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal power supplies trimmed to factory defaults.

Table 9. STANDBY MODE CURRENT CONSUMPTION

| Operating Conditions | Wakeup Source | VBAT | DC Conversion | Min | Typ | Max | Unit |
|--|---------------|--------|---------------|-----|------|-----|------|
| Clocks stopped All peripherals disabled 8 kB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K inactive | GPIO | 3.0 V | BUCK Mode | | 17 | | μA |
| | | 1.8 V | BUCK Mode | | 20 | | |
| | | 1.25 V | LDO Mode | | 26 | | |
| Clocks stopped All peripherals disabled 16 kB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K inactive | GPIO | 3.0 V | BUCK Mode | | 17.5 | | μA |
| | | 1.8 V | BUCK Mode | | 21 | | |
| | | 1.25 V | LDO Mode | | 26 | | |
| Clocks stopped All peripherals disabled 32 kB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K inactive | GPIO | 3.0 V | BUCK Mode | | 17.6 | | μA |
| | | 1.8 V | BUCK Mode | | 21 | | |
| | | 1.25 V | LDO Mode | | 26 | | |
| Clocks stopped All peripherals disabled 64 kB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K inactive | GPIO | 3.0 V | BUCK Mode | | 18 | | μA |
| | | 1.8 V | BUCK Mode | | 21 | | |
| | | 1.25 V | LDO Mode | | 26 | | |
| Clocks stopped All peripherals disabled 8 kB RAM retained 32 kHz RC32 active 32 kHz XTAL32K inactive | RTC timer | 3.0 V | BUCK Mode | | 21 | | μA |
| | | 1.8 V | BUCK Mode | | 22 | | |
| | | 1.25 V | LDO Mode | | 29 | | |
| Clocks stopped All peripherals disabled 8 kB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K active | RTC timer | 3.0 V | BUCK Mode | | 19 | | μA |
| | | 1.8 V | BUCK Mode | | 21 | | |
| | | 1.25 V | LDO Mode | | 28 | | |

Sleep Mode Current Consumption

Table 10 shows key current consumption values for Sleep Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck

mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal supplies trimmed to factory defaults.

Table 10. SLEEP MODE CURRENT CONSUMPTION

| Operating Conditions | Symbol | Wakeup Source | VBAT | DC Conversion | Min | Typ | Max | Unit |
|--|--------|---------------|--------|---------------|-----|-----|-----|------|
| Clocks stopped All peripherals disabled No RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K inactive | Ids1 | GPIO | 3.0 V | BUCK Mode | | 40 | | nA |
| | | | 1.8 V | BUCK Mode | | 50 | | |
| | | | 1.25 V | LDO Mode | | 70 | | |
| System clocks stopped All peripherals disabled No RAM retained 32 kHz RC32 active 32 kHz XTAL32K inactive | Ids2 | RTC timer | 3.0 V | BUCK Mode | | 100 | | nA |
| | | | 1.8 V | BUCK Mode | | 130 | | |
| | | | 1.25 V | LDO Mode | | 200 | | |
| System clocks stopped All peripherals disabled No RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K active | Ids3 | RTC timer | 3.0 V | BUCK Mode | | 60 | | nA |
| | | | 1.8 V | BUCK Mode | | 80 | | |
| | | | 1.25 V | LDO Mode | | 120 | | |
| System clocks stopped All peripherals disabled 8 KB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K active | Ids4 | RTC timer | 3.0 V | BUCK Mode | | 180 | | nA |
| | | | 1.8 V | BUCK Mode | | 260 | | |
| | | | 1.25 V | LDO Mode | | 430 | | |
| System clocks stopped All peripherals disabled 16 KB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K active | Ids5 | RTC timer | 3.0 V | BUCK Mode | | 220 | | nA |
| | | | 1.8 V | BUCK Mode | | 320 | | |
| | | | 1.25 V | LDO Mode | | 530 | | |
| System clocks stopped All peripherals disabled 32 KB RAM retained 32 kHz RC32 inactive 32 kHz XTAL32K active | Ids6 | RTC timer | 3.0 V | BUCK Mode | | 300 | | nA |
| | | | 1.8 V | BUCK Mode | | 440 | | |
| | | | 1.25 V | LDO Mode | | 730 | | |

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ULP Data Acquisition Subsystem Performance

Table 11 shows key current consumption values for ULP Data Acquisition Subsystem in Smart Sense Mode. Unless otherwise noted, the specifications mentioned in the table

below are valid at 25°C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal supplies trimmed to factory defaults.

Table 11. ULP DATA ACQUISITION SUBSYSTEM PERFORMANCE

| Operating Condition | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| Continuous ADC operation in Smart Sense mode with wakeup on ADC threshold Configuration/conditions: VBAT = 3 V, BUCK Mode, Successive Approximation ADC enabled and selected, XTAL32K, VREF = VBAT reference selected, ADC Fs = 256 sps, accumulation 4 samples. Processor would wake to Run mode by ADC threshold but this is not included in this measurement | | 206 | | nA |
| Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 kB RAM retained, XTAL32K, Successive Approximation ADC enabled, VREF = VBAT, ADC Fs = 1 ksps, accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM | | 2.1 | | μA |
| Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 kB RAM retained. XTAL32K, Successive Approximation ADC enabled, VREF = VDDA, ADC Fs = 1 ksps, Accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM | | 4.1 | | μA |
| Continuous Pulse Counter accumulation in Smart Sense mode, wakeup when FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 kB RAM retained, XTAL32K, Pulse Counter enabled, Pulse Count Interval 1000 ms, accumulation of 5 samples, result stored in FIFO. Processor wakes to Run mode every 5 s to transfer sample to RAM | | 348 | | nA |

Wakeup Timing Specifications

Table 12. WAKEUP TIMING SPECIFICATIONS

| Description | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--------|--|-----|------------------|-----|------|
| Cold startup – VBAT applied to entering RUN mode | | To start of startup code execution (Energy Harvesting state) | | 2.4 | | ms |
| | | To start of startup code execution (Secure state) using secure bootloader with two key certificates, one content certificate, debug port locked and application size of ~55 kB | | 236 | | |
| GPIO wakeup from Sleep mode to RUN mode, RAM execution | | To start of wakeup function execution in RAM (startup code is not executed). VDDM retained | | 1.47 (Note 6) | | ms |
| GPIO wakeup from Sleep mode to RUN mode, flash execution | | To start of startup code execution | | 1.55 (Note 6) | | ms |
| GPIO wakeup from Sleep mode to RUN mode, continuation from flash | | To start of execution from last program counter address (startup code is not executed). VDDM retained | | 1.49 (Note 6) | | ms |
| GPIO wakeup from Standby mode to RUN mode, continuation from flash | | To start of execution from last program counter address (startup code is not executed). VDDC retained | | 125 | | μs |
| GPIO wakeup from IDLE mode to RUN mode, continuation from RAM or flash | | To start of execution from last program counter address (startup code is not executed). VDDC retained | | 90 | | μs |

6. Wakeup times may vary due to system capacitance and sleep period.

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Table 13. EEMBC BENCHMARK SCORES (All RSL15 benchmark scores have been certified by EEMBC)

| Description | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--------|-----------------------|-----|------|-----|----------|
| EEMBC CoreMark | | | | 177 | | CoreMark |
| EEMBC ULPMark™ –CoreMark | | Performance | | 60.5 | | |
| | | Energy, Fixed Voltage | | 58.3 | | |
| | | Energy, Best Voltage | | 63.1 | | |
| EEMBC ULPMark™ –CoreProfile | | 1.8 V | | 1220 | | |
| | | 3 V | | 1070 | | |

RF Specifications

Table 14 shows key RF specifications. Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT ≤ 1.4 V).

Table 14. RF SPECIFICATIONS

| Description | Symbol | Conditions | Min | Typ | Max | Unit |
|---|------------------|--|------|------|------|------|
| GENERAL RADIO SPECIFICATIONS | | | | | | |
| RF Input Impedance | Z _{in} | | | 50 | | Ω |
| Input reflection coefficient | S ₁₁ | | | | -8 | dB |
| Data Rate | R _{FSK} | FSK/MSK/GFSK (OQPSK as MSK) | 62.5 | 1000 | 3000 | kbps |
| | | 4-FSK | | | 4000 | kbps |
| SYNTHESIZER SPECIFICATIONS | | | | | | |
| Frequency Range | F _{RF} | | 2360 | | 2500 | MHz |
| Rx Frequency Step | | Receive mode frequency synthesizer resolution | | | 100 | Hz |
| Tx Frequency Step | | Transmit mode frequency synthesizer resolution | | | 600 | Hz |
| PLL Settling Time | | Receive Mode | | 15 | 25 | μs |
| PLL Settling Time | | Transmit Mode | | 5 | 10 | μs |
| RECEIVE MODE SPECIFICATIONS | | | | | | |
| BLE Sensitivity LDO mode, VBAT = 1.8 V or 3.0 V Buck mode, VBAT = 1.8 V | | 1 Mbps, 0.1% BER | | -96 | | dBm |
| | | 2 Mbps, 0.1% BER | | -94 | | dBm |
| | | 500 kbps, 0.1% BER, BLE Long Range | | -98 | | dBm |
| | | 125 kbps, 0.1% BER, BLE Long Range | | -102 | | dBm |
| BLE Sensitivity Buck mode, VBAT = 3.0 V (QFN) | | 1 Mbps, 0.1% BER | | -94 | | dBm |
| | | 2 Mbps, 0.1% BER | | -91 | | dBm |
| | | 500 kbps, 0.1% BER, BLE Long Range | | -96 | | dBm |
| | | 125 kbps, 0.1% BER, BLE Long Range | | -100 | | dBm |
| Rx sensitivity degradation VSWR1:4 | | Any phase relative to 50 Ω | | 3.5 | | dB |
| RSSI effective range | | Without AGC | | 60 | | dB |
| RSSI step size | | | | 2.4 | | dB |
| Rx AGC Range | | | | 48 | | dB |
| Rx AGC Step Size | | Programmable | | 6 | | dB |
| Max usable input signal level | | 0.1% BER | | 0 | | dBm |

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Table 14. RF SPECIFICATIONS (continued)

| Description | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--------|---|------|-----|----------------|------|
| TRANSMIT MODE SPECIFICATIONS | | | | | | |
| Transmit power range | | BLE, VDDPA is required for $\geq +3$ dBm or in low voltage conditions | -17 | | +6 (Note 7) | dBm |
| Transmit power step size | | | | 1 | | dBm |
| Transmit power accuracy | | Tx power 0 dBm. Full band. Relative to the typical value. | -1.5 | | +1.5 | dBm |
| | | Tx power 3 dBm. Full band. Relative to the typical value. | -1.5 | | +1.5 | dBm |
| | | Tx power 6 dBm. Full band. Relative to the typical value. | -1.5 | | +1.5 | dBm |
| Power in 2 nd harmonic | | 0 dBm output level | | -35 | | dBm |
| Power in 3 rd harmonic | | 0 dBm output level | | -40 | | dBm |
| Power in 4 th harmonic | | 0 dBm output level | | -45 | | dBm |
| Power in 2 nd harmonic with EVB harmonic filter | | 0 dBm output level | | -55 | | dBm |
| Power in 3 rd harmonic with EVB harmonic filter | | 0 dBm output level | | -60 | | dBm |
| Power in 4 th harmonic with EVB harmonic filter | | 0 dBm output level | | -60 | | dBm |
| Tx power degradation VSWR 1:4 | | Any phase relative to 50 Ω , for 0 dBm output level | | 2.5 | | dB |

7. At +6 dBm Tx power, an antenna gain of +2.2 dBi or less must be used to ensure out-of-band regulatory emissions compliance.

Flash Specifications

Table 15. FLASH SPECIFICATIONS

| Description | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------|---------------------|-----|-----|-----|---------|
| Flash sector endurance | | Code and Data Array | 50 | | | kcycles |
| | | NVR Array | 1 | | | |
| Flash content retention period | | T = 55°C | 25 | | | years |
| Sector erase time | | | | 1 | 4 | ms |
| Mass write time | | | | | 10 | ms |

Oscillator Specifications

Table 16. 32 kHz CRYSTAL OSCILLATOR (XTAL32K)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---------------------------|---------|--|-----|--------|------|------------|
| Crystal Frequency | XTAL32K | | | 32.768 | | kHz |
| Startup time | | VBAT applied to stabilization | | 1 | 3 | s |
| Internal load | | Internal capacity to match crystal unit load capacity. Steps of 0.4 pF | 0 | | 25.2 | pF |
| External load Capacitance | | Maximum external capacity allowed (package, routing, etc.) | | | 3.5 | pF |
| Internal ESR | | | | | 100 | k Ω |
| Operating current | | Using optimal external component (low CL and ESR) | | 25 | | nA |
| Duty cycle | | | 40 | 50 | 60 | % |

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Table 17. SLOW RC OSCILLATOR (RC32)

| Parameter | Symbol | Notes | Min | Typ | Max | Unit |
|---------------------------|--------|--------------------------|-----|--------|-----|------|
| Factory trimmed frequency | RC32 | | | 32.768 | | kHz |
| Startup time | | After VBAT applied | | | 2 | ms |
| Current consumption | | Temperature comp enabled | | 120 | | nA |

Table 18. 48 MHz CRYSTAL OSCILLATOR (RFCLK)

| Parameter | Symbol | Notes | Min | Typ | Max | Unit |
|--------------------------------|--------|--|-----|-----|-----|----------|
| Crystal Frequency | RFCLK | | | 48 | | MHz |
| Startup time | | After VBAT Applied | | | 1.5 | ms |
| Recommended XTAL parameter ESR | | Equiv. Series res. | 20 | | 80 | Ω |
| Recommended XTAL parameter CL | | Differential equivalent load capacitance. The effective differential capacitance (XTAL and parasitics) must be <1 pF, the remaining being capacitance to ground (parasitic completed by on-chip load capacitance). | 6 | 8 | 10 | pF |
| Operating current | | | | 100 | | μ A |
| Duty cycle | | | 40 | | 60 | % |

NOTE: RFCLK (48 MHz crystal) must be the clock source when writing to Flash.

Table 19. FAST RC OSCILLATOR (RCCLK)

| Parameter | Symbol | Notes | Min | Typ | Max | Unit |
|---|--------|---------------------------------|------|-----|-----|---------|
| Fast RC Oscillator Output Frequency | RCCLK | 3 MHz Output | | 3 | | MHz |
| | | 12 MHz Output | | 12 | | |
| | | 24 MHz Output | | 24 | | |
| Fast RC Oscillator temperature coefficient (Note 8) | | T = 0 to +45°C, 3 MHz Output | -1.5 | | 1.5 | % |
| | | T = -40 to +85°C, 3 MHz Output | -3.5 | | 3.5 | % |
| | | T = 0 to +45°C, 12 MHz Output | -5 | | 5 | % |
| | | T = -40 to +85°C, 12 MHz Output | -15 | | 15 | % |
| | | T = 0 to +45°C, 24 MHz Output | -10 | | 10 | % |
| | | T = -40 to +85°C, 24 MHz Output | -25 | | 25 | % |
| Duty cycle | | | 40 | 50 | 60 | % |
| Current consumption | | 3 MHz Output | | 5 | | μ A |
| | | 12 MHz Output | | 18 | | μ A |
| | | 24 MHz Output | | 38 | | μ A |
| Startup time | | After VBAT Applied | | | 100 | μ s |

8. For setting of $V_{CC} = 1.2$ V

Analog Comparator Specifications (ACOMP)

Table 20. ANALOG COMPARATOR SPECIFICATIONS (ACOMP)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---------------------|--------|------------------------|-----|-----|------|------|
| Input voltage range | | Rail-to-rail input | 0 | | VBAT | V |
| Input offset | | Full common mode range | -10 | | 10 | mV |
| Hysteresis | | Low power setting | 40 | | 90 | mV |
| | | Normal setting | 40 | | 110 | |
| | | High speed setting | 40 | | 220 | |
| Comparator delay | | Low power setting | | 120 | | μs |
| | | Normal setting | | 1.5 | | μs |
| | | High speed setting | | 0.2 | | μs |
| Current consumption | | Low power setting | | 10 | | nA |
| | | Normal setting | | 1.5 | | μA |
| | | High speed setting | | 18 | | μA |

Successive Approximation ADC (SAR ADC) Specifications

Table 21. SUCCESSIVE APPROXIMATION ADC (SAR ADC) SPECIFICATIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------------|--------|---|-------|-----|-------|------------|
| ADC reference voltage | VREF | VBAT selected as reference VREF | 1.8 | | 3.6 | V |
| | | GPIO[9] selected as reference VREF | 1.8 | | VDDO | V |
| Resolution | | | | 12 | | Bits |
| Input voltage range | | | 0 | | VREF | V |
| Differential input voltage range | | | -VREF | | VREF | V |
| Sampling rate | | VREF ≥ 2.5 V | | | 2 | Msp/s |
| | | VREF 2.0 V to 2.5 V | | | 0.5 | Msp/s |
| | | VREF 1.8 V to 2.0 V | | | 0.125 | Msp/s |
| LSB weight | | 12 bits resolution at VREF = VBAT = 3.6 V | | 1.6 | | mV |
| Absolute gain error | | | -2 | | +2 | % |
| INL | | | -4 | | 4 | LSB |
| DNL | | | -1.5 | | 1.5 | LSB |
| Offset | | After calibration | -5 | | 5 | LSB |
| Gain error | | After calibration | -1 | | 1 | % |
| Noise | | RMS noise in LSB for a constant input voltage | | | 2 | LSBrms |
| Input capacitance | | | | 1 | | pF |
| Array calibration time | | | | 650 | | cycles |
| Current consumption | | | | 26 | | μA / Msp/s |

Low Speed ADC Converter (LSAD) Specifications

Table 22. LOW SPEED ADC CONVERTER (LSAD) SPECIFICATIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|----------------------|--|--------|-----|------|------|
| Resolution | ADC _{RES} | | 8 | 12 | 14 | bits |
| Precision | ADC _{PRES} | 0–50°C | –20 | | 20 | mV |
| Input voltage range | ADC _{RANGE} | | 0 | | 2 | V |
| INL | ADC _{INL} | | –2 | | +2 | mV |
| DNL | ADC _{DNL} | | –1 | | +1 | mV |
| Channel sampling frequency | ADC _{CH_SF} | 8 channels are converted sequentially, ADC running at 50 kHz | 0.0195 | | 6.25 | kHz |

NOTE: All LSAD parameters are for SLOWCLK at 1 MHz.

Table 23. DAC SPECIFICATIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------------|--------------------|---|-----|-----|------------|------|
| Output voltage range | V _{out} | Cannot exceed VDDO | 0.1 | | VDDA – 0.2 | V |
| Output voltage step size | V _{steps} | | | 16 | | mV |
| Output current | I _{out} | Max current results in a typ 50 mV drop on the pad, VDDO > 2.2V | 0 | | 10 | μA |

Temperature Sensor Specifications

Table 24. TEMPERATURE SENSOR SPECIFICATIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--------|--------------------------------------|-----|------|-----|--------|
| Accuracy potential | | Requires calibration by the customer | –2 | | 2 | °C |
| Temperature sensor output voltage @ 25°C | | Uncalibrated | 0.9 | 0.95 | 1 | V |
| Temperature sensor gain @ 25°C | | | | 21.3 | | LSB/°C |
| Startup time | | From enable to specified accuracy | | 100 | 200 | μs |
| Active current consumption | | | | | 10 | μA |

Pulse Counter Specifications

Table 25. PULSE COUNTER SPECIFICATIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------|--------|---------------------------------|-----------------------|-----|-------|-------|
| Pulse width | | | >1 sensor clock cycle | | | cycle |
| Pulse count duration | | Using accumulation to reach max | 0.976 | | 16000 | ms |

GPIO Interface Specifications

Table 26. GPIO INTERFACE SPECIFICATIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|--|-----------|--------------|-------------|-----|----------------------|------|----|
| Voltage level for HIGH Input | VIH | | 0.75 x VDDO | | VDDO +0.3 | V | |
| Voltage level for LOW Input | VIL | | -0.3 | | 0.25 x VDDO (Note 9) | V | |
| Voltage level for HIGH Output | VOH | | VDDO - 0.4 | | | V | |
| Voltage level for LOW Output | VOL | | | | 0.4 | V | |
| Voltage at GPIO selected as LSAD input | Vlsad | | VSSA - 0.3 | | 2 | V | |
| Drive Strength (Note 10) | IOH / IOL | VDDO = 3.3 V | Drive = 0 | | 3.4 | | mA |
| | | | Drive = 1 | | 6.8 | | mA |
| | | | Drive = 2 | | 13.5 | | mA |
| | | | Drive = 3 | | 20.2 | | mA |
| | | VDDO = 1.8 V | Drive = 0 | | 2.0 | | mA |
| | | | Drive = 1 | | 4.0 | | mA |
| | | | Drive = 2 | | 8.0 | | mA |
| | | | Drive = 3 | | 12.1 | | mA |
| Weak Pull-up Resistor | | | 250 | | kΩ | | |
| Strong Pull-up Resistor | | | 10 | | kΩ | | |
| Pull-down Resistor | | | 250 | | kΩ | | |

9. For VDDO < 1.8 V, VIL Max is 0.23 x VDDO.

10. Maximum accumulated current from all GPIO should not exceed 200 mA.

TYPICAL CONNECTION DIAGRAMS

It is recommend to have external access to a UART for general diagnostics and for wired communication during Bluetooth certification. It is also recommend to have a method to load new firmware during Bluetooth certification. Firmware can be loaded by any method such as the Serial Wire Debug (SWD) with pins SWDIO, SWCLK, VDDO (IO voltage domain) and a ground connection. Two GPIO must be externally accessible for the UART. The UART GPIO do not need to be permanently dedicated to UART in

the final product as temporary provisions can be made to repurpose the GPIO during certification, as long there is no impact to RF performance.

BUCK Mode Operation

Figure 6 shows RSL15 external components and connections for BUCK Mode operation with GPIO Levels at GND and VBAT.

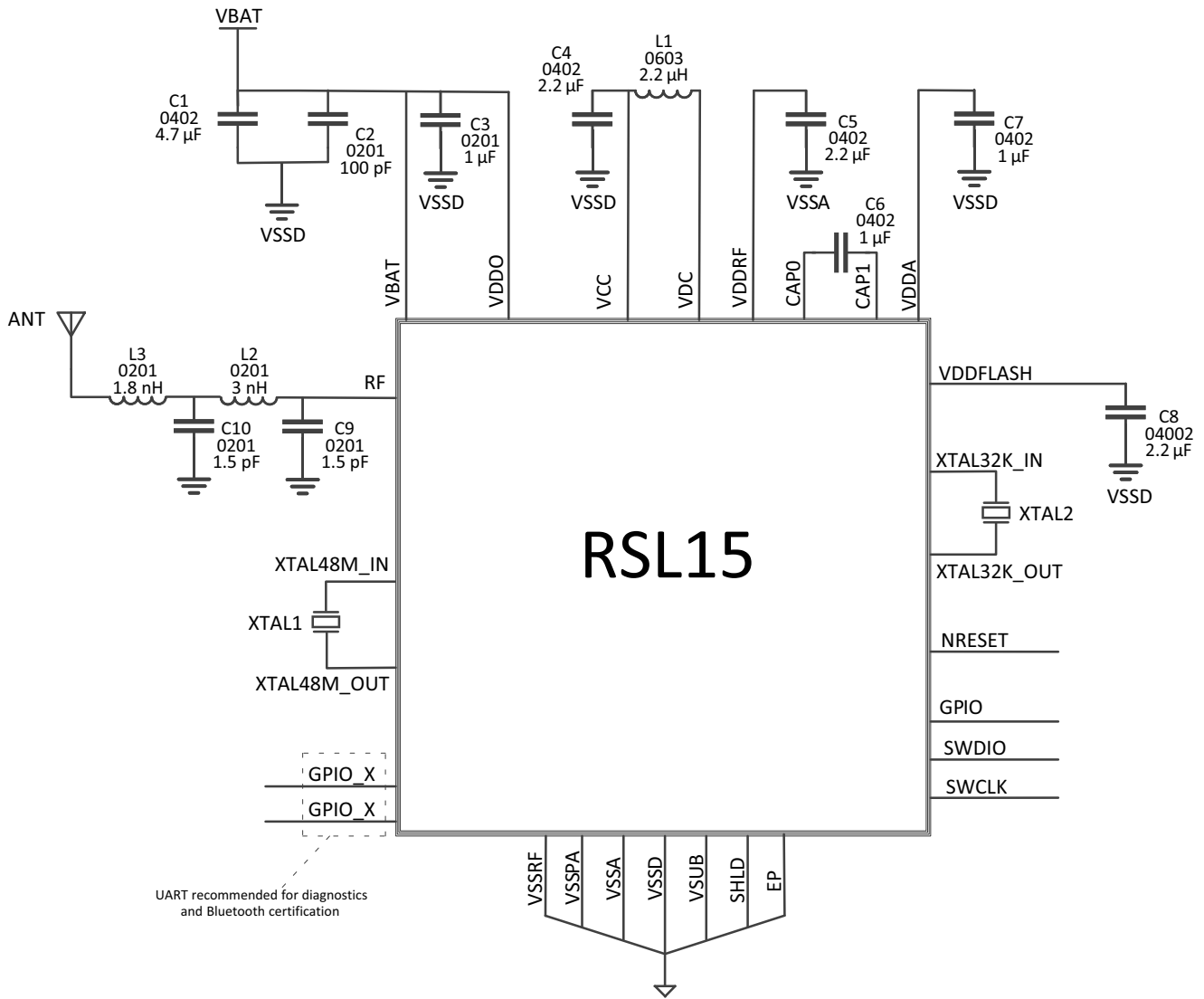


Figure 6. RSL15 BUCK Mode Connection Diagram, VDDO = VBAT

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LDO Mode Operation

Figure 7 shows RSL15 external components and connections for LDO Mode operation with GPIO Levels at GND and VBAT.

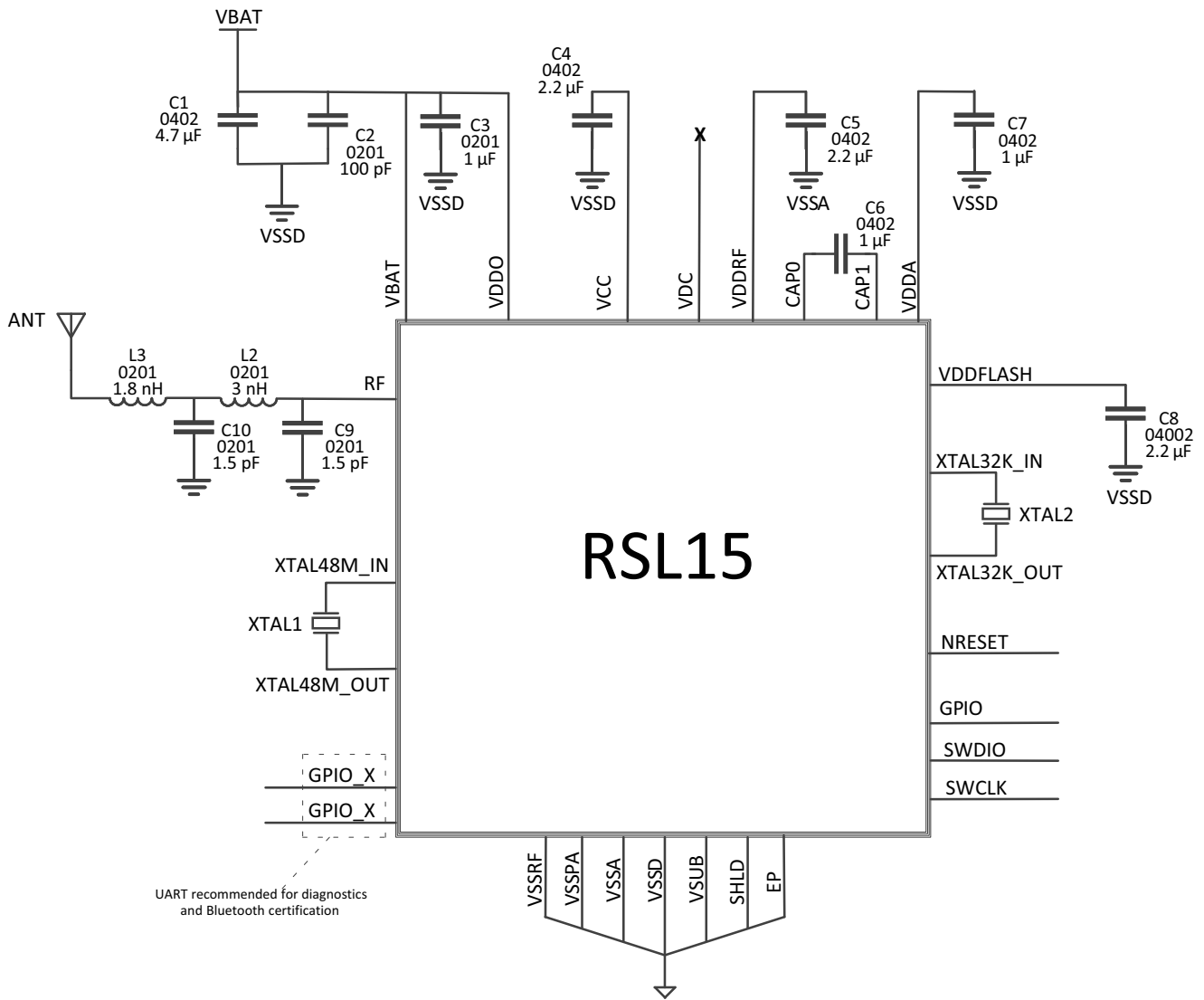


Figure 7. RSL15 LDO Mode Connection Diagram, VDDO = VBAT

External Component Overview

Table 27. RECOMMENDED EXTERNAL COMPONENTS

| Components | Function | Recommended Typical Value | Nominal Tolerance |
|-----------------|------------------------------------|--|-------------------|
| C1, C2 | VBAT decoupling | 4.7 μ F // 100 pF (Note 11) | \pm 20% |
| C3 | VDDO decoupling | 1 μ F | \pm 20% |
| C4 | VCC decoupling | 2.2 μ F – GRM155C80J225KE95D, Murata – AMK105BJ225, Taiyo Yuden | \pm 20% |
| C5 | VDDRF decoupling | 2.2 μ F | \pm 20% |
| C6 | Pump capacitor for the charge pump | 1 μ F | \pm 20% |
| C7 | VDDA decoupling | 1 μ F | \pm 20% |
| C8 | VDDFLASH decoupling | 2.2 μ F | \pm 20% |
| | | | |
| L1 | DC–DC converter inductance | 2.2 μ H (See Table 28 below) | \pm 20% |
| XTAL1 | XTAL for 48 MHz oscillator | – 416F48022IKR, CTS Frequency Controls – 8Q–48.000MEEV–T, TXC Corporation, Taiwan | |
| XTAL2 | XTAL for 32 kHz oscillator | – 9HT12–32.768KDZF–T, TXC Corporation – MC–306, Epson – CM8V–T1A, Micro Crystal Switzerland | |
| C9, C10, L2, L3 | External harmonic filter | C9 1.5 pF / C10 1.5 pF \pm 0.25 pF, C0G/NP0, Murata GRM0335C L2 3 nH / L3 1.8 nH \pm 0.1 nH, Murata LQP03TN (Note 12) | |

NOTE: Capacitors C1 to C8 recommendations:

Multilayer ceramic caps with nominal voltage 6.3 V (to reduce capacitance drop due to DC biasing effect), ESR < 0.2 Ω over frequency range 100k – 10MHz, Type X5R with max \pm 15% variation over temperature range so \pm 35% total capacitance tolerance.

11. The recommended decoupling capacitance uses 2 capacitors with the values specified.

12. For improved harmonic performance in environments where RSL15 is operating in close proximity to smartphones or base stations, FBAR filters such as the Broadcom ACPF–7924 can be applied instead of the suggested discrete harmonic filter.

Table 28. RECOMMENDED DC–DC CONVERTER INDUCTANCE TABLE

| Manufacturer | Part Number | Case Size | Comments |
|--------------|----------------|--------------------------------------|---|
| Murata | LQM18PN2R2MGHD | 0603 SMD with $T_{max} = 1.0$ mm | Default inductor used on evaluation board. |
| Murata | LQM21PZ2R2MC0 | 0805 SMD with $T_{max} = 0.55$ mm | Recommended inductor for Vbat > 3.0V to minimize RX sensitivity degradation in Buck mode versus LDO mode operation. A low–profile, AEC–Q200 option. |

NOTE: Recommended inductor ESR is 0.2 Ω Typ, 0.5 Ω Max and saturation current 200 mA Min.

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PIN DEFINITIONS

QFN40 Pin Out

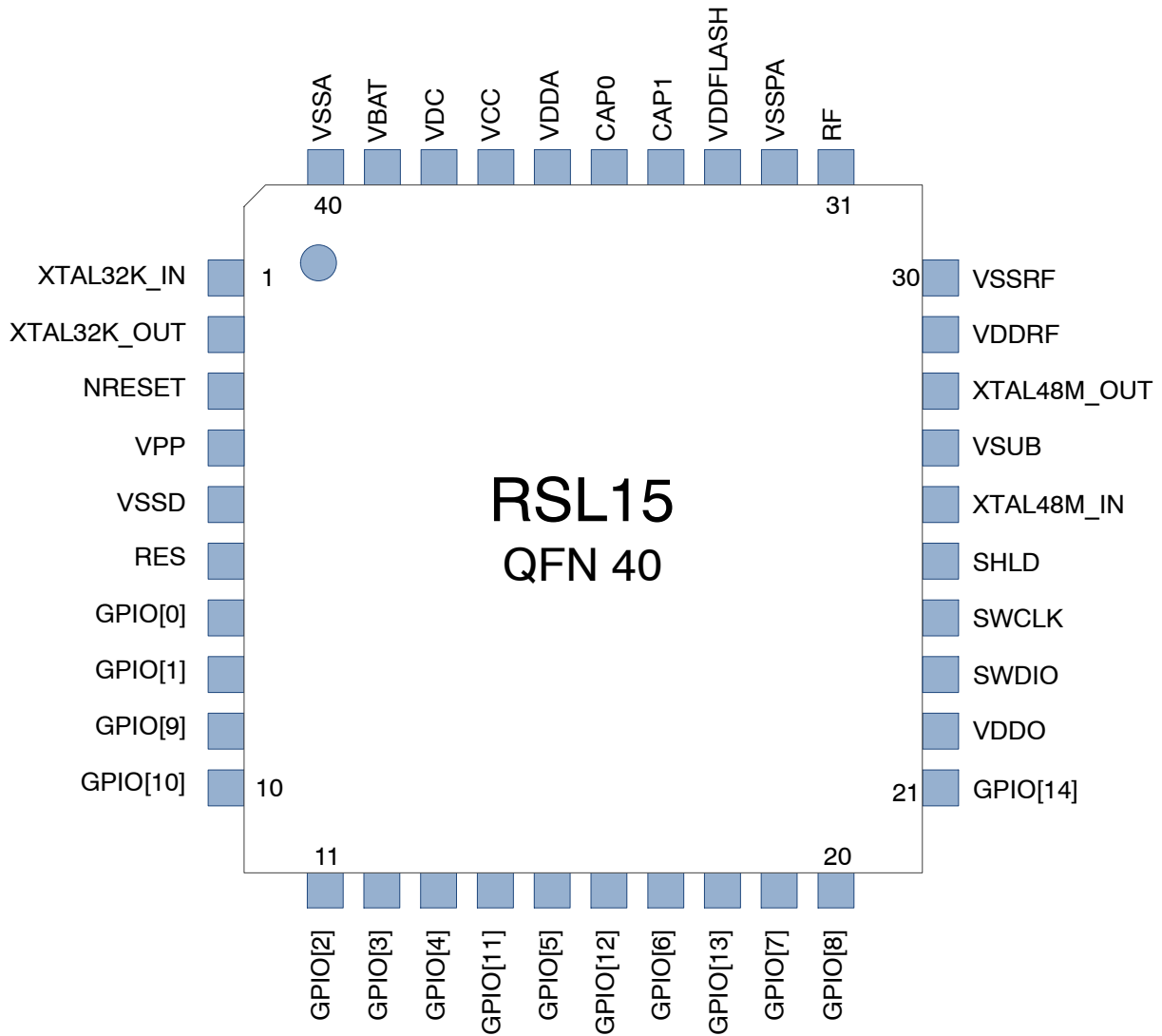


Figure 8. QFN40 Pin Out

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Pin Definition and Multiplexing

RSL15 has very flexible pad multiplexing capabilities. Most functions are available on any GPIO. Table 29: Pin Definition lists all pins and their functionality while Table 30: GPIO Multiplexing shows all multiplexed functions available on the GPIO.

Legend:

I = input; O = output; P = power;

Pull: PU = pull up; PD = pull down;

Table 29. PIN DEFINITION AND MULTIPLEXING

| Pad Name | Description | Power Domain | Type | Pull | Pad #, QFN |
|-------------|--|--------------|------|-------|---------------|
| XTAL32K_IN | Input pin for 32 kHz XTAL | VBAT | | | 1 |
| XTAL32K_OUT | Output pin for 32 kHz XTAL | VBAT | | | 2 |
| NRESET | Reset pin | VDDO | I | PU | 3 |
| VPP | Flash high voltage access, do not connect (NC) | | P | | 4 |
| VSSD | Core logic ground | | P | | 5 |
| RES | RESERVED, do not connect | | | | 6 |
| GPIO[0] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 7 |
| GPIO[1] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 8 |
| GPIO[9] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 9 |
| GPIO[10] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 10 |
| GPIO[2] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 11 |
| GPIO[3] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 12 |
| GPIO[4] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 13 |
| GPIO[11] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 14 |
| GPIO[5] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 15 |
| GPIO[12] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 16 |
| GPIO[6] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 17 |
| GPIO[13] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 18 |
| GPIO[7] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 19 |
| GPIO[8] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 20 |
| GPIO[14] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | 21 |
| GPIO[15] | General Purpose I/O, see Table 30: GPIO Multiplexing | VDDO | I/O | PU/PD | Not Available |
| VDDO | Digital I/O voltage supply | VDDO | P | | 22 |
| SWDIO | For Serial Wire Debug (SWD) or JTMS for JTAG-DP | VDDO | | PU | 23 |
| SWCLK | For Serial Wire Debug (SWD) or JTCK for JTAG-DP | VDDO | | PU | 24 |

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Table 29. PIN DEFINITION AND MULTIPLEXING (continued)

| Pad Name | Description | Power Domain | Type | Pull | Pad #, QFN |
|-------------|--|--------------|------|------|------------|
| SHLD | Connect to ground | | | | 25 |
| XTAL48M_IN | Input pin for 48 MHz XTAL | | | | 26 |
| VSUB | Substrate ground (RF) | | P | | 27 |
| XTAL48M_OUT | Output pin for 48 MHz XTAL | | | | 28 |
| VDDRF | LDO for RF | | P | | 29 |
| VSSRF | RF analog ground | | P | | 30 |
| RF | RF signal input/output (Antenna) | | I/O | | 31 |
| VSSPA | Ground for RF PA LDO | VDDA | P | | 32 |
| VDDFLASH | LDO for Flash | VDDA | P | | 33 |
| CAP1 | Charge pump capacitor | VDDA | | | 34 |
| CAP0 | Charge pump capacitor | VDDA | | | 35 |
| VDDA | Charge pump output for analog and flash supplies | VDDA | P | | 36 |
| VCC | VCC regulator decoupling | VBAT | P | | 37 |
| VDC | DC-DC output voltage to external LC filter | VBAT | P | | 38 |
| VBAT | Battery input voltage | VBAT | P | | 39 |
| VSSA | Analog ground | | P | | 40 |
| EP | Exposed pad, connect to ground | | | | |

Table 30. GPIO MULTIPLEXING

| GPIO | Mode | Description |
|------|--|---|
| 0 | RTC_CLK_OUTPUT (Note 14) | RTC clock output |
| 0:3 | RTC_CLK_INPUT | Input for external RTC clock source |
| | WAKEUP_SOURCE | Wakeup source from low power modes |
| | INTERRUPT_SOURCE | Interrupt source |
| | PULSE_COUNTER_INPUT | Pulse Counter Input |
| 2 | JTAG_TDO JTAG | Test Data Out |
| 3 | JTAG_TDI JTAG | Test Data In |
| 4 | JTAG_TRST JTAG | Test Reset |
| 4 | ACS-PWM (Note 13) | Always On PWM in the Analog Control Subsystem (ACS) |
| 7 | SDAC_OUTPUT | SDAC output |
| 9 | SAR_ADC SUPPLY & REFERENCE | SAR ADC voltage supply and reference (VREF) |
| 0:15 | SAR_ADC_INPUT LSAD_INPUT ACOMP_INPUT AOUT | SAR_ADC_INPUT LSAD_INPUT ACOMP_INPUT AOUT |
| 0:15 | SLOWCLK (output) SYSCLK (output) USRCLK (output) RCCLK (output) SWCLK (output) EXTCLK (output/input) STANDBYCLK (output) SENSORCLK (output) | Clocking |

Table 30. GPIO MULTIPLEXING (continued)

| GPIO | Mode | Description |
|------|--|-------------|
| 0:15 | UART0_RX UART0_TX / LIN0_TX LIN_RX SPI0_MOSI/DATA0 SPI0_MISO/DATA1 SPI0_DATA2 SPI0_DATA3 SPI0_CS SPI0_CLK SPI1_MOSI/DATA0 SPI1_MISO/DATA1 SPI1_DATA2 SPI1_DATA3 SPI1_CS SPI1_CLK I2C0_SCL I2C0_SDA I2C1_SCL I2C2_SDA PWM0 PWM1 PWM2 PWM3 PWM4 PWM0_INV PWM1_INV PWM2_INV PWM3_INV PWM4_INV PCM_SER1 PCM_SER0 PCM_FRAME PCM_CLK | Interfaces |

13. ACS-PWM has an equivalent 500 Ohm series resistor at the output.

14. RTC_CLK_OUTPUT output level is at VCC in Sleep Mode.

PCB LAYOUT GUIDELINES

1. Decoupling capacitors should be placed as close to the related balls as possible
2. Differential output signals should be routed as symmetrically as possible
3. Analog input signals should be shielded as well as possible
4. Pay close attention to the parasitic coupling capacitors
5. Special care should be made for PCB design in order to obtain good RF performance
6. Multi-layer PCB should be used with a keep-out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip's pin to the supply source
8. Digital signals should not be routed close to the crystal or the power supply lines
9. Proper DC-DC component placement and layout is critical to RX sensitivity performance in DC-DC mode. Minimize parasitic capacitance and inductance on the VDC node as much as possible.
10. [QFN only]: Ground EP by vias to a ground plane and/or through at least two VSS pins to PCB surface ground.
11. [QFN only]: Connect SHLD pin to EP, and connect SHLD to an external ground trace shielding XTAL48M_IN from SWCLK.

PACKAGE MARKING INFORMATION

Chip Identification

System identification is used to identify different system components. For the RSL15 chip, the key identifier components and values are as follows:

Chip Family: 0x0B

Chip Version: 0x02

Chip Major Revision: 0x02

ELECTROSTATIC DISCHARGE (ESD) SENSITIVE DEVICE

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high-energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

SOLDER INFORMATION

The RSL15 QFN package is constructed with all RoHS compliant material and should be reflowed accordingly.

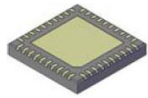
This device is Moisture Sensitive Class MSL1 and must be stored and handled accordingly. Re-flow according to IPC/JEDEC standard J-STD-020C, Joint Industry Standard: Re-flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For more information, see SOLDERRM/D available from <http://onsemi.com>.

EXPORT CONTROL CLASSIFICATION NUMBER (ECCN)

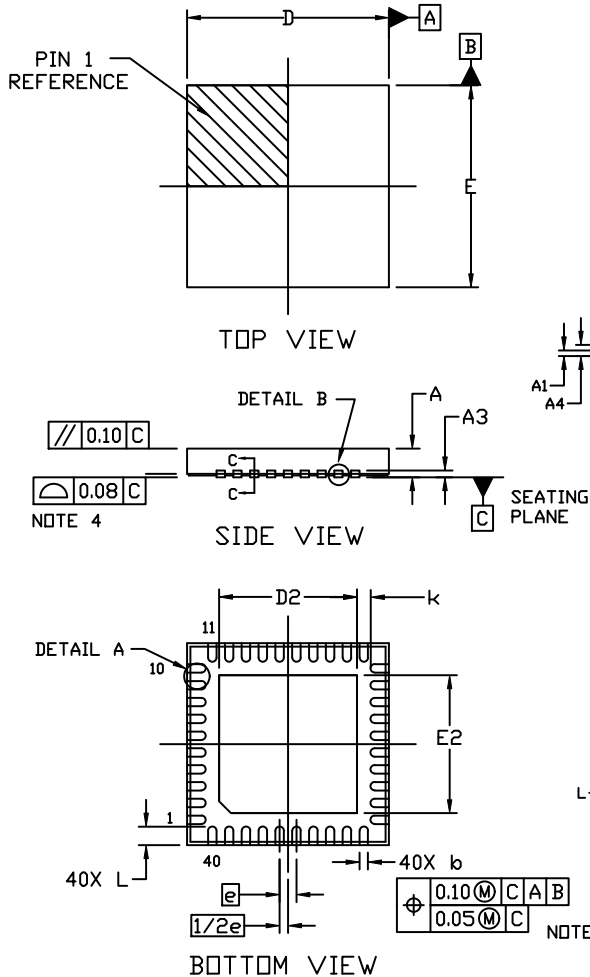
The ECCN designation for RSL15 is 5a991.g .

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



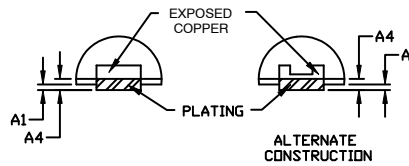
QFNW40 6x6, 0.5P CASE 484BC ISSUE O

DATE 14 FEB 2022

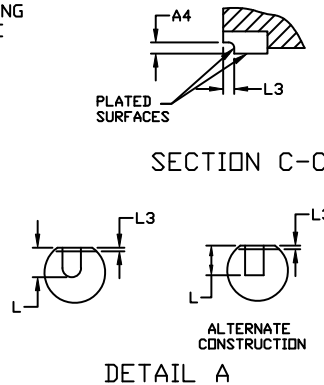


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

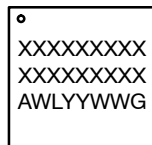


SECTION C-C



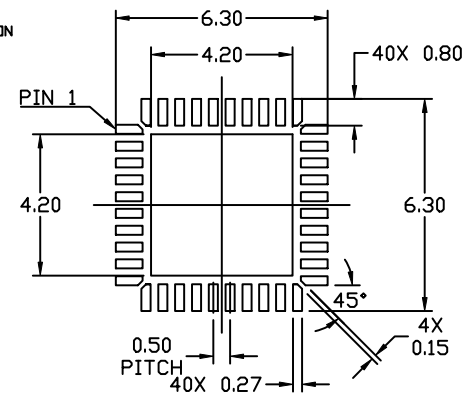
| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NDM. | MAX. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | --- | --- | 0.05 |
| A3 | 0.20 REF | | |
| A4 | 0.10 | --- | --- |
| b | 0.20 | 0.25 | 0.30 |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 4.00 | 4.10 | 4.20 |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 4.00 | 4.10 | 4.20 |
| e | 0.50 BSC | | |
| K | 0.25 | --- | --- |
| L | 0.30 | 0.40 | 0.50 |
| L3 | 0.05 | --- | --- |

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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