

NCS2553

標準画質再生フィルタ付き3チャンネル・ビデオ・アンプ

説明

NCS2553は、6次バターワース標準画質再生フィルタ付き3チャンネル高速ビデオ・アンプです。

3チャンネルすべてが、全コンポーネント・ビデオ信号およびRGBビデオ信号、またはコンポジット信号およびSビデオ信号のいずれかに対応できます。全チャンネルがDCまたはAC結合信号を受け入れることができます。AC結合の場合、内部クランプが採用されます。出力は、ACおよびDC結合150Ω負荷をドライブできます。

ほとんどのビデオ・プロセッサに組み込まれている、大部分のデジタル-アナログ・コンバータ(DAC)と互換性があるように設計されています。

特長

- 3個の6次標準画質8MHzフィルタ
- 内部固定ゲイン=6dB
- ACまたはDC結合入力
- ACまたはDC結合出力
- 集積化レベル・シフト
- 動作電圧 +5V
- SOIC-8パッケージで供給
- 鉛フリー・デバイス

アプリケーション

- デジタル・セットトップ・ボックス
- DVD/ビデオ・プレーヤおよび関連機器
- SD-TV
- ビデオ・オン・デマンド(VOD)
- ビデオ・レコーダ



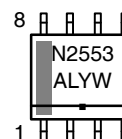
ON Semiconductor®

<http://onsemi.com>



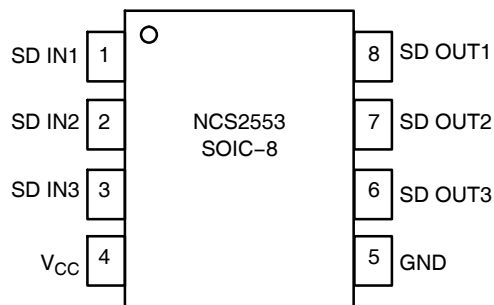
SOIC-8 NB
D SUFFIX
CASE 751

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
NCS2553DG	SOIC-8 (Pb-Free)	98 Units / Rail
NCS2553DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCS2553

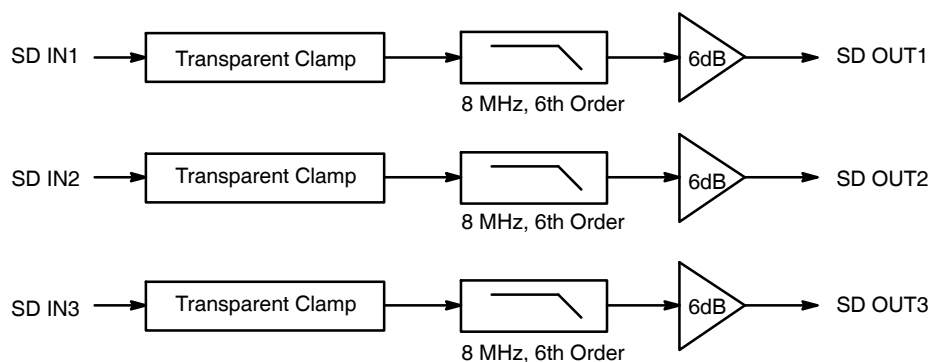


Figure 1. Block Diagram

PIN FUNCTION AND DESCRIPTION

Pin	Name	Type	Description
1	IN1	Input	Video Input 1 for Video Signal featuring a frequency bandwidth compatible with Standard Definition Video (8 MHz) – Channel 1
2	IN2	Input	Video Input 2 for Video Signal featuring a frequency bandwidth compatible with Standard Definition Video (8 MHz) – Channel 2
3	IN3	Input	Video Input 3 for Video Signal featuring a frequency bandwidth compatible with Standard Definition Video (8 MHz) – Channel 3
4	VCC	Power	Device Power Supply Voltage: +5 V
5	GND	GND	Connected to Ground
6	OUT3	Output	SD Video Output 3 – Channel 3
7	OUT2	Output	SD Video Output 2 – Channel 2
8	OUT1	Output	SD Video Output 1 – Channel 1

ATTRIBUTES

Characteristics	Value
ESD	
Human Body Model	All Pins (Note 1) 8 kV
Machine Model	Pins 1 to 5 (Note 2) 400 V
	All Output Pins (Note 2) 800 V
Moisture Sensitivity (Note 3)	Level 1
Flammability Rating – Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in

1. Human Body Model (HBM): R = 1500 Ω , C = 100 pF
2. Machine Model (MM)
3. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltages	V_{CC}	$-0.35 \leq V_{CC} \leq 5.5$	Vdc
Input Voltage Range	V_I	$-0.3 \leq V_I \leq V_{CC}$	Vdc
Input Differential Voltage Range	V_{ID}	$V_I \leq V_{CC}$	Vdc
Output Current	I_O	50	mA
Maximum Junction Temperature (Note 4)	T_J	150	°C
Operating Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	112.7	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

最大消費電力

安全に散逸可能な最大電力は、関連する接合部温度の上昇によって制限されます。

プラスチック・パッケージの場合、最大安全接合部温度は150°Cです。瞬時的に最大値を超えた場合、ダイ温度が低下するとすぐに適切な回路動作が回復します。デバイスを長期間「過熱」状態に置くと、デバイス・バーンアウトが発生する可能性があります。適切な動作を保証するには、ディレーティング曲線を順守することが大切です。

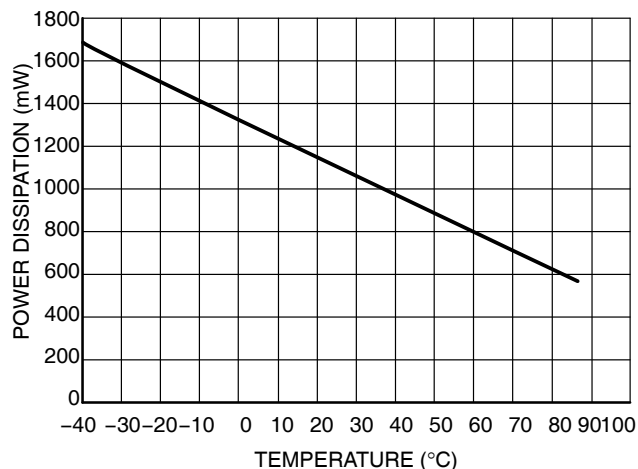


Figure 2. Power Dissipation vs Temperature

NCS2553

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $0.1\ \mu\text{F}$ AC coupled inputs, $R_{\text{source}} = 37.5\ \Omega$, $220\ \mu\text{F}$ AC coupled outputs into $150\ \Omega$ load, referenced to $400\ \text{kHz}$, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range		4.75	5.0	5.25	V
I_{CC}	Power Supply Current	No Load		23	30	mA
V_{IN}	Input Common Mode Voltage Range	Referenced to GND if DC-Coupled	GND		1.4	
PSRR	Power Supply Rejection	DC (All Channels)		-50		dB

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than $500\ \text{lfpm}$. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $0.1\ \mu\text{F}$ AC coupled inputs, $R_{\text{source}} = 37.5\ \Omega$, $220\ \mu\text{F}$ AC coupled outputs into $150\ \Omega$ load, referenced to $400\ \text{kHz}$, unless otherwise specified)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
A_{VOL}	Voltage Gain (Note 5)	$V_{IN} = 1\ \text{V}$ (All Channels)	5.8	6.0	6.2	dB
BW	Low Pass Filter Bandwidth	-1 dB (Note 6)	5.5	7.2		MHz
		-3 dB		9.0		MHz
A_R	Stop-Band Attenuation (Rejection)	at $27\ \text{MHz}$		45		dB
dG	Differential Gain			0.3		%
$d\theta$	Differential Phase			0.6		°
THD	Total Harmonic Distortion	$V_{OUT} = 1.8\ V_{PP}$ @ $1\ \text{MHz}$		0.4		%
X_{talk}	Channel-to-Channel Crosstalk	$V_{OUT} = 1.8\ V_{PP}$ @ $1\ \text{MHz}$		-60		dB
SNR	Signal-to-Noise Ratio	NTSC-7, $100\ \text{kHz}$ to $4.2\ \text{MHz}$ (Note 7)		75		dB
Tpd	Propagation Delay	Input-to-Output, $4.5\ \text{MHz}$		60		nsec
ΔGD	Group Delay Variation from $100\ \text{kHz}$ to $8\ \text{MHz}$			27		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than $500\ \text{lfpm}$. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. 100% of tested IC fit to the bandwidth tolerance.
6. Guaranteed by design and characterization.
7. $\text{SNR} = 20 \times \log(714\ \text{mV/RMS Noise})$

TYPICAL CHARACTERISTICS

$V_{CC} = +5.0\text{ V}$, $R_{source} = 37.5\ \Omega$, $T_A = 25^\circ\text{C}$, $0.1\ \mu\text{F}$ AC-coupled inputs, $220\ \mu\text{F}$ AC-coupled outputs into $150\ \Omega$ referenced to $400\ \text{kHz}$, all channels, unless otherwise specified

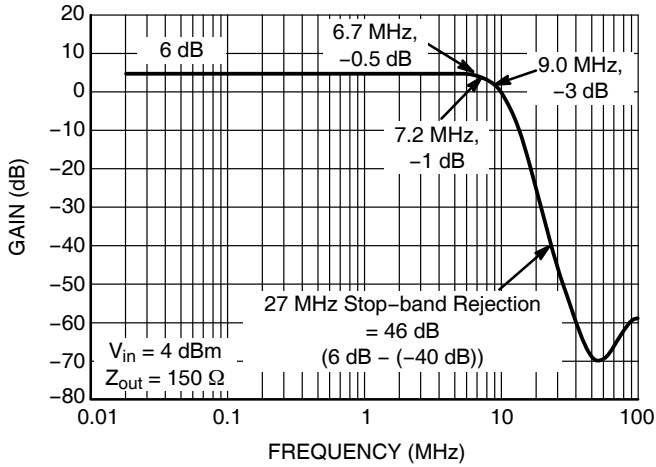


Figure 3. Frequency Response

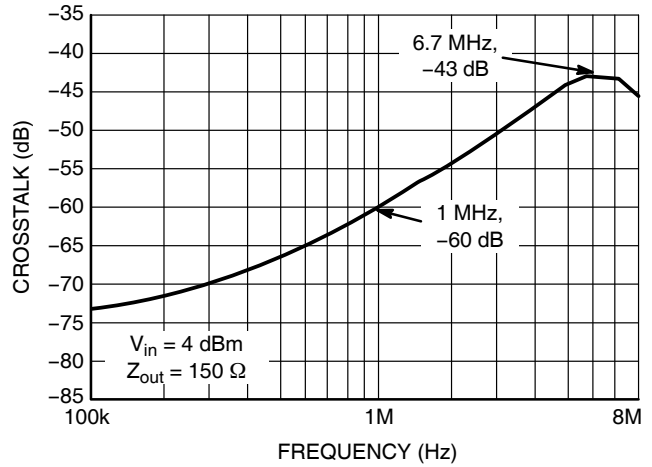


Figure 4. Channel-to-Channel Crosstalk

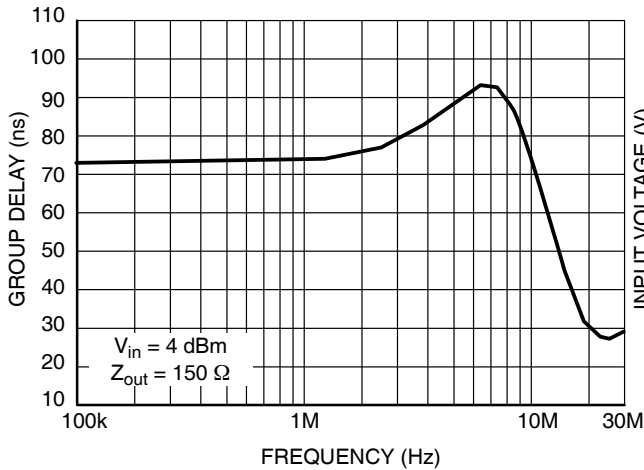


Figure 5. Group Delay

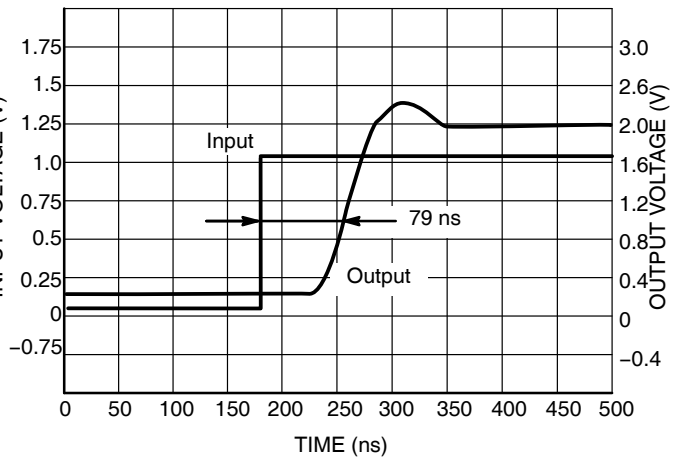


Figure 6. Propagation Delay

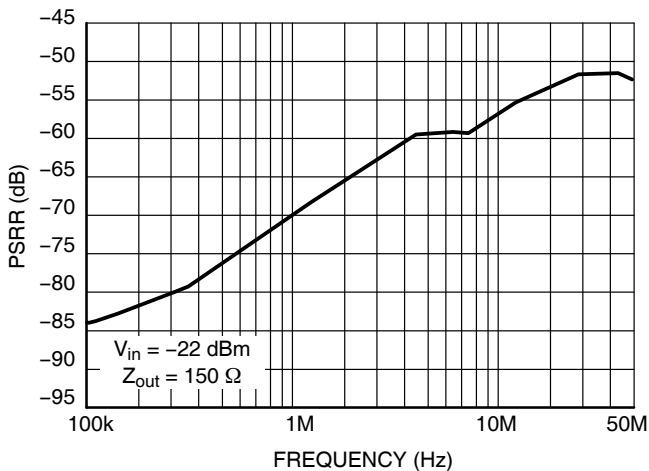


Figure 7. PSRR vs Frequency (No Bypass Capacitor)

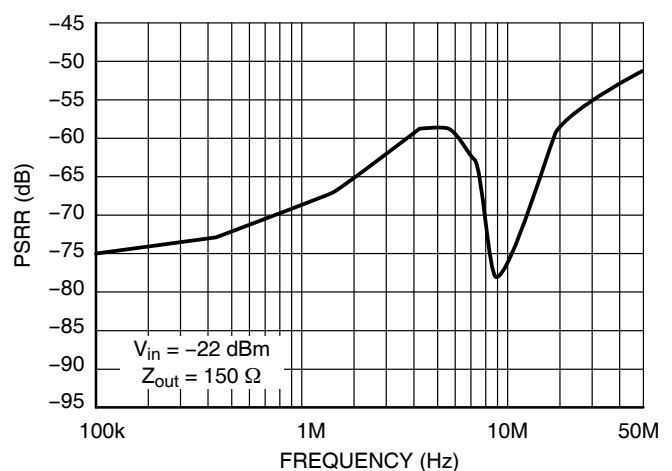


Figure 8. PSRR vs. Frequency (Bypass Capacitor)

TYPICAL CHARACTERISTICS

$V_{CC} = +5.0\text{ V}$, $R_{source} = 37.5\ \Omega$, $T_A = 25^\circ\text{C}$, $0.1\ \mu\text{F}$ AC-coupled inputs, $220\ \mu\text{F}$ AC-coupled outputs into $150\ \Omega$ referenced to $400\ \text{kHz}$, all channels, unless otherwise specified

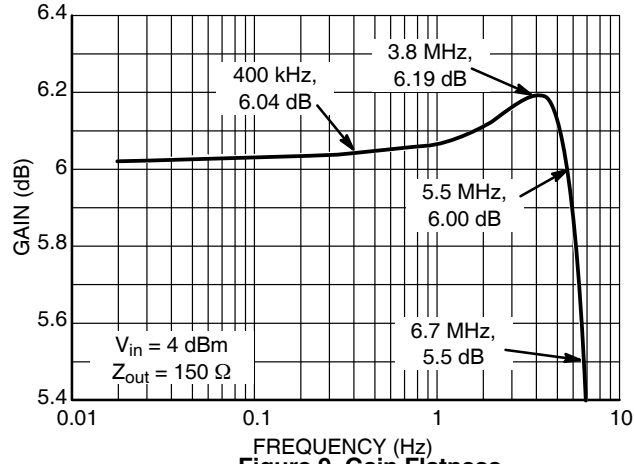


Figure 9. Gain Flatness

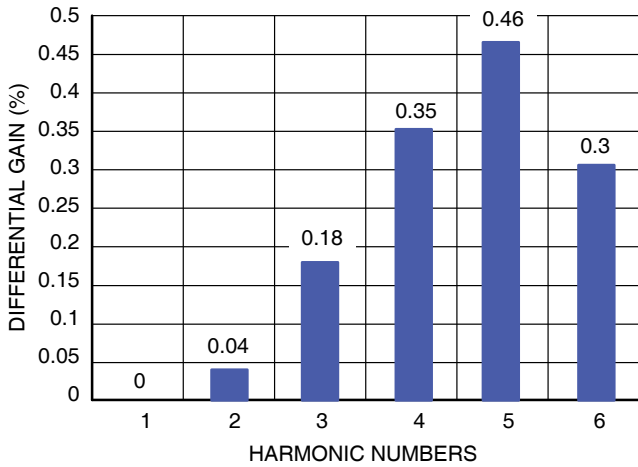


Figure 10. Differential Gain (NTSC 5 Steps Input Signal)

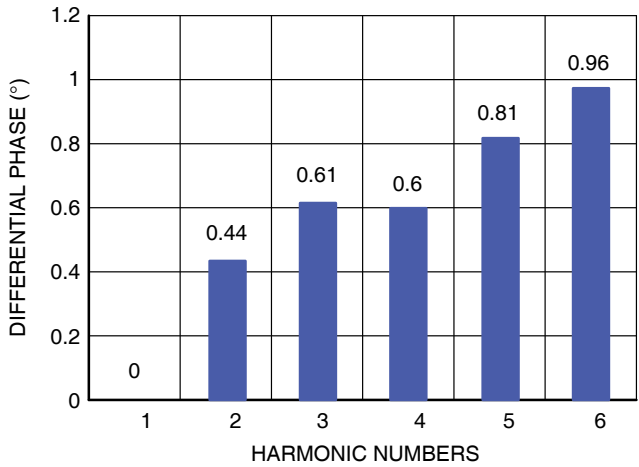


Figure 11. Differential Phase (NTSC 5 Steps Input Signal)

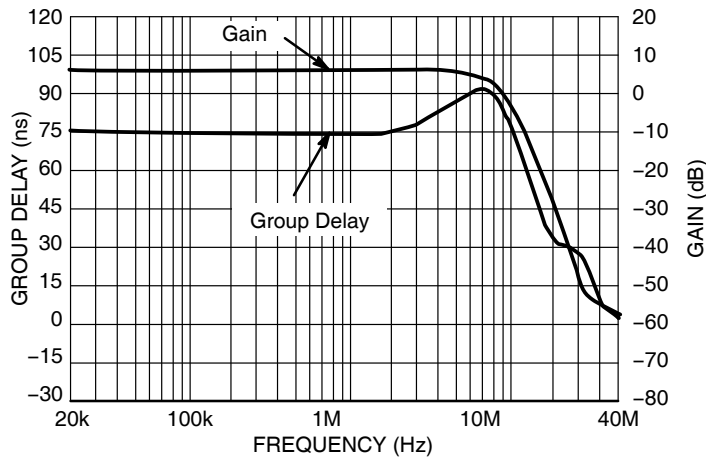


Figure 12. Normalized Frequency Response and Group Delay vs. Frequency

NCS2553トリプル・ビデオ・ドライバは、CVBS、Sビデオ、480i/525i & 576i/625i規格の要件に対応する標準画像ビデオ・アプリケーション向けに最適化されています。高いチャンネル間クロストークの絶縁によって、3チャンネルすべてが同一仕様で、同様な動作をすることが保証されます。各チャンネルは入力から出力に内部電圧-電圧ゲイン2を提供し、ディスクリート・アプローチ（独立したオペアンプを使用）の場合に通常必要な外付け部品点数を削減します。内部レベル・シフタを採用し、約280mVのオフセットを追加して、出力電圧を高くしています。これによって、同期パルスのクリップを防止し、150Ωのビデオ負荷に対する

DC結合出力を可能にします。また、NCS2553は、チャンネルごとに8MHzの3dB周波数帯域幅を持つ6次バターワース・フィルタを内蔵しています。これによって、ビデオDACにより発生するエイリアスや望ましくないオーバーサンプリングの影響を取り除くことができます。同様に、ADCを使用したDVDレコーダのケースでは、このアンチエイリアシング・フィルタ（再生フィルタ）は画質の問題を回避し、EMI干渉に起因する寄生信号を除去するのに役立ちます。

チップ内で各チャンネルに対して内蔵ダイオードのようなクランプが使用され、AC結合動作モードをサポートします。入力信号が0V以下になると、クランプが有効になります。

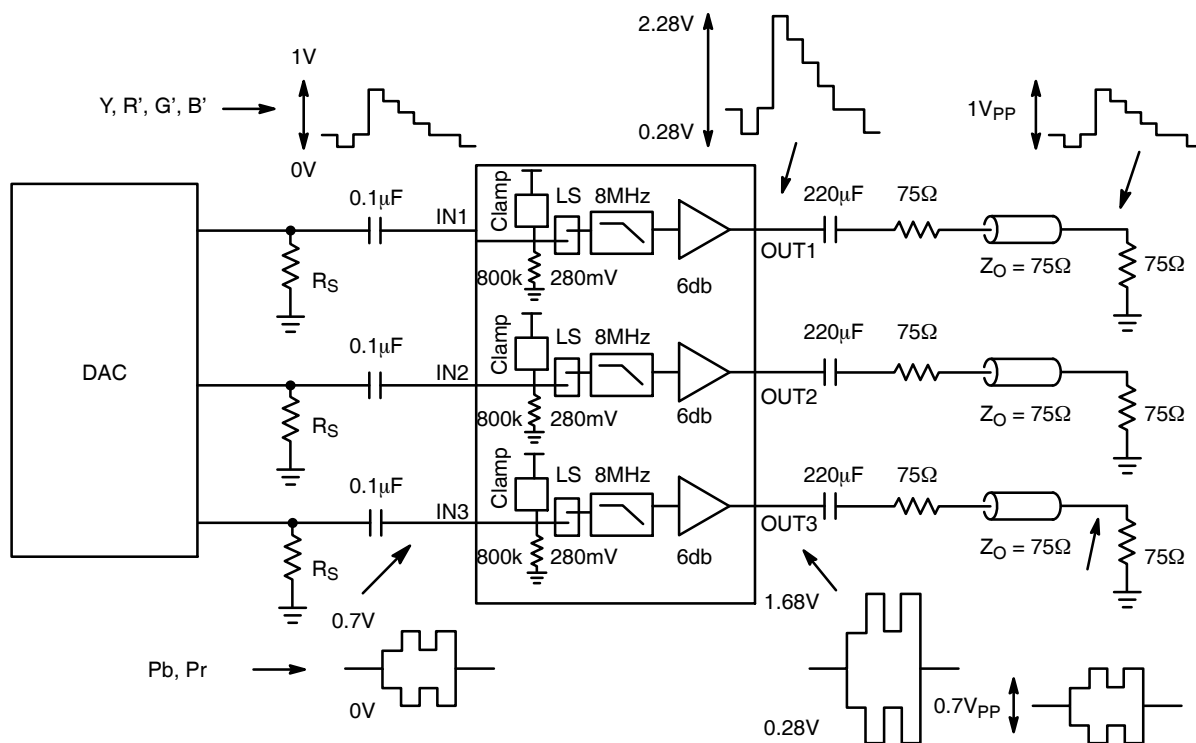


Figure 13. AC-Coupled Inputs and Outputs

Figure 13に、DACから来る外部ビデオ・ソースが入力および出力でAC結合される例を示します。しかし、内蔵トランスペアレント・クランプおよびレベル・シフタのために、デバイスは基本的にDAC出力信号レベルのハイおよびローに応じて、またビデオ・ドライバの入力コモン・モード電圧にどのように適合するかに応じて、異なる構成モードで動作することができます。構成が入力および出力でのDC結合の場合、0.1µFおよび220µFのカップリング・コンデンサは使用されず、クランプは非アクティブになります。この構成には外付け部品点数が少なく、比較的lowコストであるという大きな利点があります。

例えば、入力信号振幅が0~1.4Vの範囲を超えたり、ビデオ・ソースで必要になる場合、入力はAC結合されます。状況によっては、プルアップ抵抗とプルダウン抵抗またはプルアップ抵抗のみ（標準7.5MΩと内部800kΩプルダウン）を追加して、クランプを非アクティブすることによって、信号を自動バイアスしなければならない場合があります。

出力のAC結合構成には、出力カップリング・コンデンサの容量が低すぎる場合に、デバイスがビデオ・ラインやフィールド傾き問題に対してより敏感になるという欠点がありますが、DCグランド・ループをなくす利点があります。場合によっては、公称220µFのコンデンサ値を増やす必要があります。

NCS2553

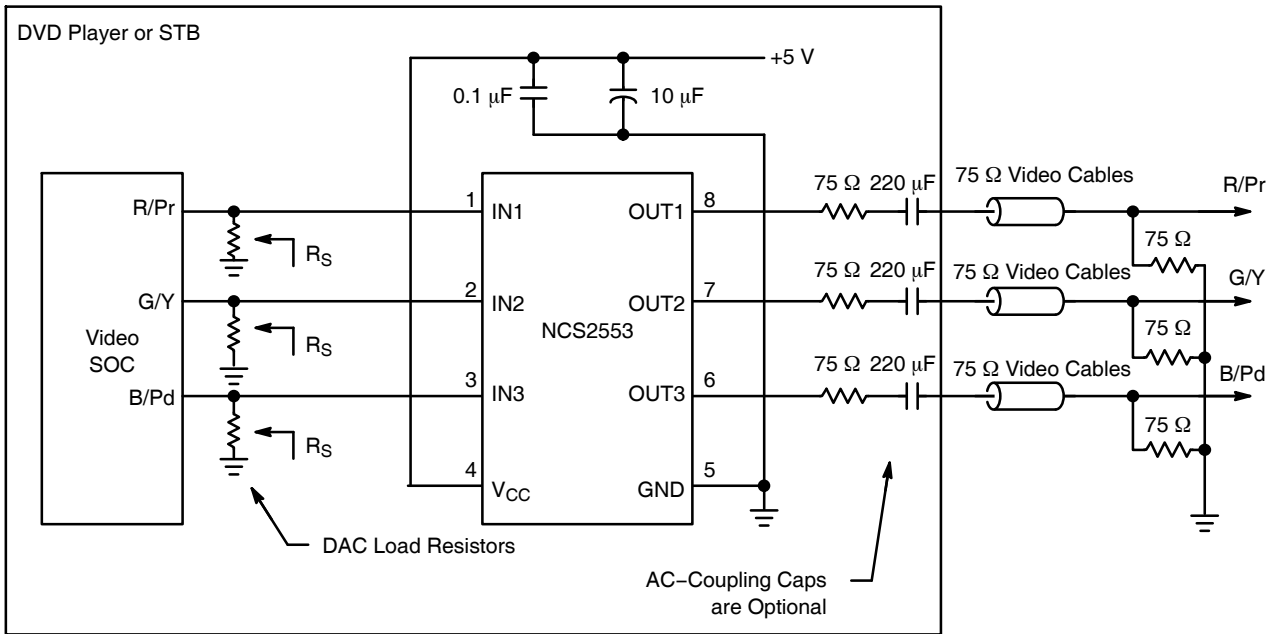


Figure 14. Typical Application Circuit

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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