NCN4555

1.8 V/3 V SIMカード電源およびレベル・シフタ

NCN4555は、SIMカードと外部マイクロコントローラまたはMPU間で電圧を変換するように設計されたレベル・シフタ・アナログ回路です。内蔵LDO型DC−DCコンバータにより、NCN4555は1.8 Vおよび3.0 VのSIMカードのドライブに使用できます。このデバイスはISO7816−3スマート・カード・インタフェース規格、GSM 11.11および関連規格(11.12および11.18)、3Gモバイル要件(IMT−2000/3G UICC規格)に準拠しています。$\overline{\text{STOP}}$ピンを使用して、低電流シャットダウン・モードを起動して、バッテリ寿命を延ばすことができます。カードの電源電圧(SIM_V_{CC})は、1本のピン(MOD_V_{CC})を使用して選択されます。

特長

- 1.8 Vまたは3.0 V動作のSIMカードをサポート
- LDOは1.8 Vおよび3.0 Vで50 mAを超える電流を供給可能
- 両方向のI/Oピンに対する内蔵プルアップ抵抗
- SIMピンでの7kVを超えるESD保護(人体モデル)を規定したISO−7816仕様に準拠し、すべてのピンを完全にESD保護
- 最大5MHz超のクロックをサポート
- 低プロフィール3x3 QFN−16パッケージ
- 鉛フリー・デバイス*

代表的アプリケーション

- 2G、2.5G、および3G携帯電話用SIMカード・インタフェース回路
- 識別モジュール
- スマート・カード・リーダ
- ワイヤレスPCカード

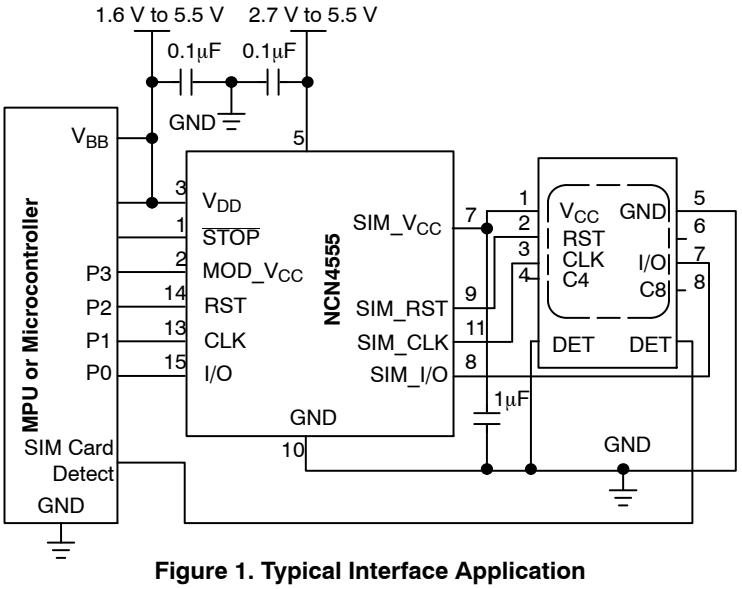

Figure 1. Typical Interface Application

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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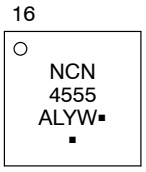
MARKING DIAGRAM

QFN−16
MN SUFFIX
CASE 488AK



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCN4555MNG	QFN−16 (Pb−Free)	123 Units / Rail
NCN4555MNR2G	QFN−16 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

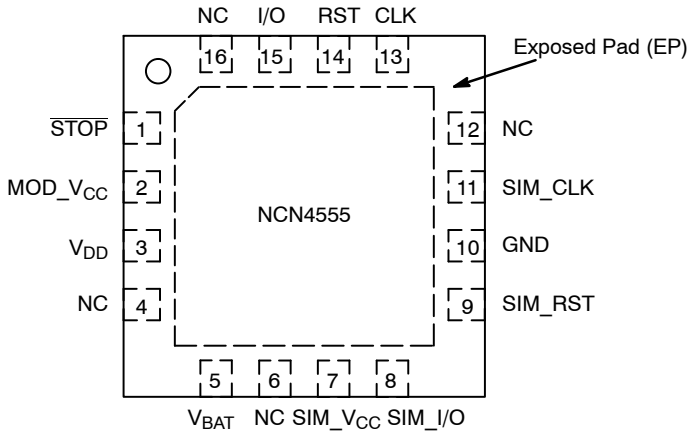


Figure 2. QFN−16 Pinout (Top View)

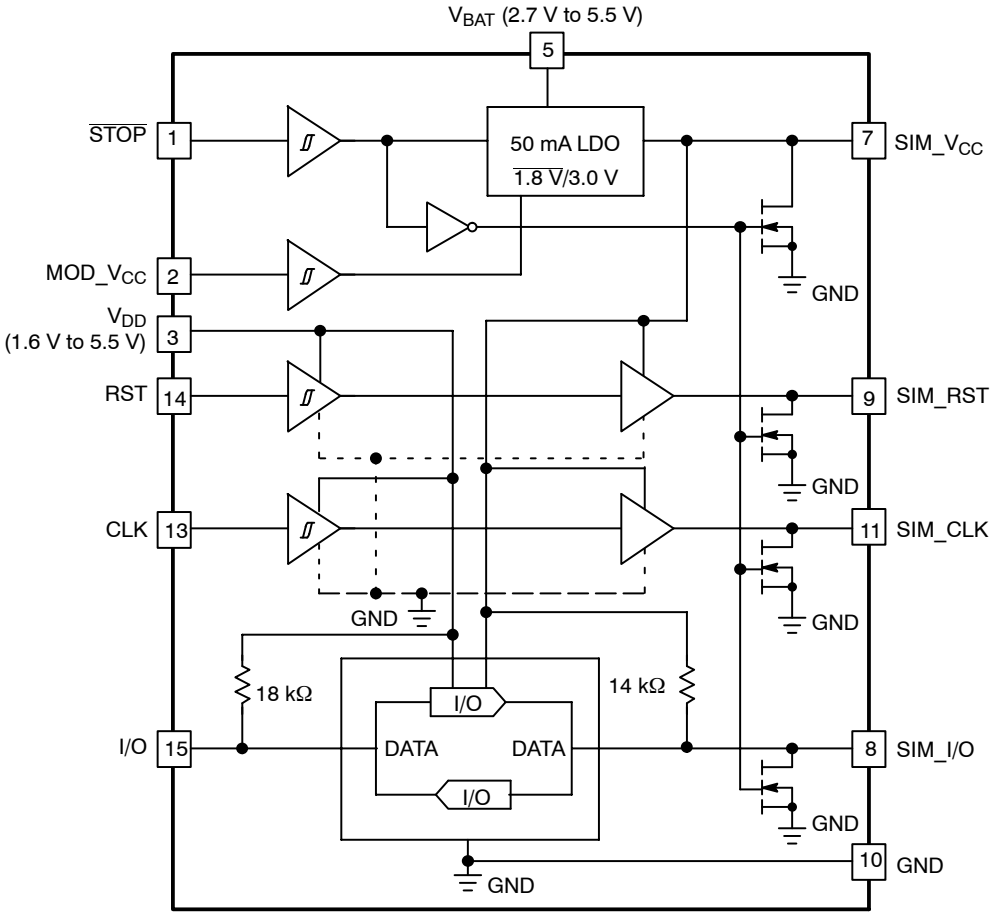


Figure 3. NCN4555 Block Diagram

PIN DESCRIPTIONS

PIN	Name	Type	Description
1	$\overline{\text{STOP}}$	INPUT	Power Down Mode pin: $\overline{\text{STOP}}$ = Low → Low current shutdown mode activated $\overline{\text{STOP}}$ = High → Normal Operation A Low level on this pin resets the SIM interface, switching off the SIM_V_{CC}.
2	MOD_V_{CC}	INPUT	The signal present on this pin programs the SIM_V_{CC} value: MOD_V_{CC} = Low → SIM_V_{CC} = 1.8 V MOD_V_{CC} = High → SIM_V_{CC} = 3 V
3	V_{DD}	POWER	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the microprocessor. A 0.1 μF capacitor shall be used to bypass the power supply voltage. When V_{DD} is below 1.1 V typical the SIM_V_{CC} is disabled. The NCN4555 comes into a shutdown mode.
4	NC		No Connect
5	V_{BAT}	POWER	DC−DC converter supply input. The input voltage ranges from 2.7V up to 5.5V. This pin has to be bypass by a 0.1 μF capacitor.
6	NC		No Connect
7	SIM_V_{CC}	POWER	This pin is connected to the SIM card power supply pin. An internal LDO converter is programmable by the external MPU to supply either 1.8 V or 3.0 V output voltage. An external 1.0 μF minimum ceramic capacitor recommended must be connected across SIM_V_{CC} and GND. During a normal operation, the SIM_V_{CC} voltage can be set to 1.8 V followed by a 3.0 V value, or can start directly to any of these two values.
8	SIM_I/O	INPUT/ OUTPUT	This pin handles the connection to the serial I/O of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the micro controller. A 14 kΩ (typical) pullup resistor provides a High impedance state for the SIM card I/O link.
9	SIM_RST	OUTPUT	This pin is connected to the RESET pin of the card connector. A level translator adapts the external Reset (RST) signal to the SIM card.
10	GND	GROUND	This pin is the GROUND reference for the integrated circuit and associated signals. Care must be taken to avoid voltage spikes when the device operates in a normal operation.
11	SIM_CLK	OUTPUT	This pin is connected to the CLOCK pin of the card connector. The CLOCK (CLK) signal comes from the external clock generator, the internal level shifter being used to adapt the voltage defined for the SIM_V_{CC}.
12	NC		No Connect
13	CLK	INPUT	The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max values defined by the specification (typically 50%). The built−in level shifter translates the input signal to the external SIM card CLK input.
14	RST	INPUT	The RESET signal present at this pin is connected to the SIM card through the internal level shifter which translates the level according to the SIM_V_{CC} programmed value.
15	I/O	INPUT/ OUTPUT	This pin is connected to an external microcontroller or cellular phone management unit. A bidirectional level translator adapts the serial I/O signal between the smart card and the external controller. A built−in constant 18 kΩ (typical) resistor provides a high impedance state when not activated.
16	NC		No Connect

ATTRIBUTES

Characteristics	Values
ESD protection HBM, SIM card pins (7, 8, 9, 10 & 11) (Note 1) HBM, All other pins (Note 1) MM, SIM card pins (7, 8, 9, 10 & 11) (Note 2) MM, All other pins (Note 2) CDM, SIM card pins (7, 8, 9, 10 & 11) (Note 3) CDM , All other pins (Note 3)	 > 7 kV > 2 kV > 600 V > 200 V > 2 kV > 600 V
Moisture sensitivity (Note 4) QFN−16	Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. Human Body Model, R = 1500 Ω, C = 100 pF.
2. Machine Model.
3. CDM, Charged Device Model.
4. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 5)

Rating	Symbol	Value	Unit
LDO Power Supply Voltage	V_{BAT}	$-0.5 \le V_{BAT} \le 6$	V
Power Supply from Microcontroller Side	V_{DD}	$-0.5 \le V_{DD} \le 6$	V
External Card Power Supply	SIM_V_{CC}	$-0.5 \le$ SIM_$V_{CC} \le 6$	V
Digital Input Pins	V_{in} I_{in}	$-0.5 \le V_{in} \le V_{DD} + 0.5$ but < 6.0 ±5	V mA
Digital Output Pins	V_{out} I_{out}	$-0.5 \le V_{out} \le V_{DD} + 0.5$ but < 6.0 ±10	V mA
SIM card Output Pins	V_{out} I_{out}	$-0.5 \le V_{out} \le$ SIM_V_{CC} + 0.5 but < 6.0 15 (internally limited)	V mA
QFN−16 Low Profile package Power Dissipation @ T_A = + 85°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta JA}$	 440 90	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+125	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C

POWER SUPPLY SECTION (−40°C to +85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
5	V_{BAT}	Power Supply	2.7		5.5	V
5	I_{VBAT}	Operating current – I_{CC} = 0 mA (Note 6)		22	30	μA
5	I_{VBAT_SD}	Shutdown current – $\overline{STOP}$= Low (Note 7)			3.0	μA
3	V_{DD}	Operating Voltage	1.6		5.5	V
3	I_{VDD}	Operating Current – f_{CLK} = 1 MHz (Note 8)		7.0	12	μA
3	I_{VDD_SD}	Shutdown Current – $\overline{STOP}$ = Low			1.0	μA
3	V_{DD}	Undervoltage Lockout	0.6		1.5	V
7	SIM_V_{CC}	MOD_V_{CC} = High, V_{BAT} = 3.0 V, I_{SIM_VCC} = 50 mA MOD_V_{CC} = High, V_{BAT} = 3.3 V to 5.5 V, I_{SIM_VCC} = 0 mA to 50 mA MOD_V_{CC} = Low, V_{BAT} = 2.7 V to 5.5 V, I_{SIM_VCC} = 0 mA to 50 mA	 2.8 1.7	2.8 3.0 1.8	 3.2 1.9	V V V
7	$I_{SIM\_VCC\_SC}$	Short –Circuit Current – SIM_V_{CC} shorted to ground , T_A=25°C			175	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. As long as $V_{BAT} - V_{DD} \leq 2.5$ V. For $V_{BAT} - V_{DD} > 2.5$ V the maximum value increases up to 35 μA (typical being in the +25 μA range).
7. As long as $V_{BAT} - V_{DD} \leq 2.5$ V.
8. Guaranteed by design over the operating temperature range specified.

DIGITAL INPUT/OUTPUT SECTION CLOCK, RESET, I/O, $\overline{STOP}$, MOD_V_{CC}

Pin	Symbol	Rating	Min	Typ	Max	Unit
1,2, 13, 14, 15	V_{in}	Input Voltage Range ($\overline{STOP}$, MOD_V_{CC}, RST, CLK, I/O)	0		V_{DD}	V
	I_{IH} & I_{IL}	Input Current ($\overline{STOP}$, MOD_V_{CC}, RST, CLK)	−100		100	nA
13, 14	V_{IH} V_{IL}	High Level Input Voltage (RST, CLK) Low Level Input Voltage (RST, CLK)	0.7 * V_{DD} (Note 9)		V_{DD} 0.4	V V
1, 2	V_{IH}	High Level Input Voltage ($\overline{STOP}$, MOD_V_{CC})	0.7 * V_{DD} (Note 9)		V_{DD}	V
	V_{IL}	Low Level Input Voltage ($\overline{STOP}$, MOD_V_{CC})	0		0.4	V
15	$V_{OH\_I/O}$ $V_{OL\_I/O}$ I_{IH} I_{IL}	High Level Output Voltage (SIM_I/O = SIM_V_{CC}, $I_{OH\_I/O}$ = −20 μA) Low Level Output Voltage (SIM_I/O = 0 V, $I_{OH\_I/O}$ = 200 μA) High Level Input Current (I/O) Low Level Input Current (I/O)	0.7 * V_{DD} 0 −20		V_{DD} 0.4 20 1.0	V V μA mA
15	$R_{pu\_I/O}$	I/0 Pullup Resistor	12	18	24	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. If 1.6 V ≤ V_{DD} ≤ 1.8 V then V_{IHmin} = 1.26 V.

SIM INTERFACE SECTION (Note 10)

Pin	Symbol	Rating	Min	Typ	Max	Unit
9	SIM_RST	SIM_V_{CC} = +3.0 V (MOD_V_{CC} = High) Output RESET V_{OH} @ I_{sim_rst} = −20 μA Output RESET V_{OL} @ I_{sim_rst} = +200 μA Output RESET Rise Time @ Cout = 30 pF Output RESET Fall Time @ Cout = 30 pF SIM_V_{CC} = +1.8 V (MOD_V_{CC} = Low) Output RESET V_{OH} @ I_{sim_rst} = −20 μA Output RESET V_{OL} @ I_{sim_rst} = +200 μA Output RESET Rise Time @ Cout = 30 pF Output RESET Fall Time @ Cout = 30 pF	 0.9 * SIM_V_{CC} 0 0.9 * SIM_V_{CC} 0		 SIM_V_{CC} 0.4 1 1 SIM_V_{CC} 0.4 1 1	 V V μs μs V V μs μs
11	SIM_CLK	SIM_V_{CC} = +3.0 V (MOD_V_{CC} = High) Output Duty Cycle Max Output Frequency Output V_{OH} @ I_{sim_clk} = −20 μA Output V_{OL} @ I_{sim_clk} = +200 μA Output SIM_CLK Rise Time @ Cout = 30 pF Output SIM_CLK Fall Time @ Cout = 30 pF SIM_V_{CC} = +1.8 V (MOD_V_{CC} = Low) Output Duty Cycle Max Output Frequency Output V_{OH} @ I_{sim_clk} = −20 μA Output V_{OL} @ I_{sim_clk} = +200 μA Output SIM_CLK Rise Time @ Cout = 30 pF Output SIM_CLK Fall Time @ Cout = 30 pF	 40 5 0.9 * SIM_V_{CC} 0 40 5 0.9 * SIM_V_{CC} 0		 60 SIM_V_{CC} 0.4 18 18 60 SIM_V_{CC} 0.4 18 18	 % MHz V V ns ns % MHz V V ns ns
8	SIM_I/O	SIM_V_{CC} = +3.0 V (MOD_V_{CC} = High) Output V_{OH} @ I_{SIM_IO} = −20 μA, $V_{I/O} = V_{DD}$ Output V_{OL} @ I_{SIM_IO} = +1 mA, $V_{I/O}$ = 0 V SIM_I/O Rise Time @ C_{out} = 30 pF SIM_I/O Fall Time @ C_{out} = 30 pF SIM_V_{CC} = +1.8 V (MOD_V_{CC} = High) Output V_{OH} @ I_{SIM_IO} = −20 μA, $V_{I/O} = V_{DD}$ Output V_{OL} @ I_{SIM_IO} = +1.0 mA, $V_{I/O}$ = 0 V SIM_I/O Rise Time @ C_{out} = 30 pF SIM_I/O Fall Time @ C_{out} = 30 pF	 0.8 * SIM_V_{CC} 0 0.8 * SIM_V_{CC} 0		 SIM_V_{CC} 0.4 1 1 SIM_V_{CC} 0.3 1 1	 V V μs μs V V μs μs
8	$R_{pu\_SIM\_I/O}$	Card I/O Pullup Resistor	10	14	18	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. All the dynamic specifications (AC specifications) are guaranteed by design over the operating temperature range.

TYPICAL CHARACTERISTICS

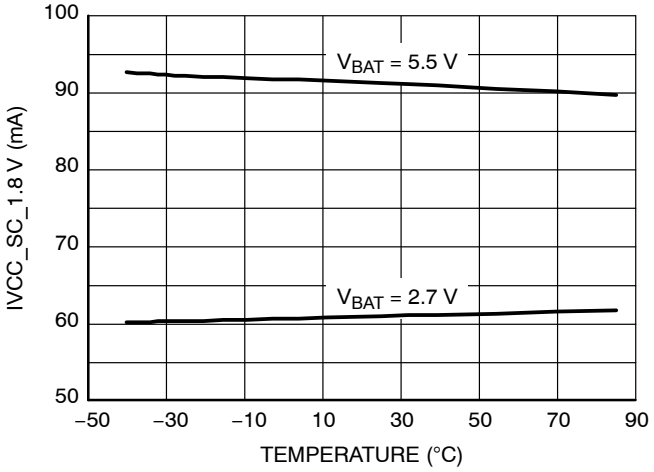


Figure 4. Short Circuit Current IV_{CC}_SC vs Temperature at SIM_V_{CC} = 1.8 V (MOD_V_{CC} = LOW)

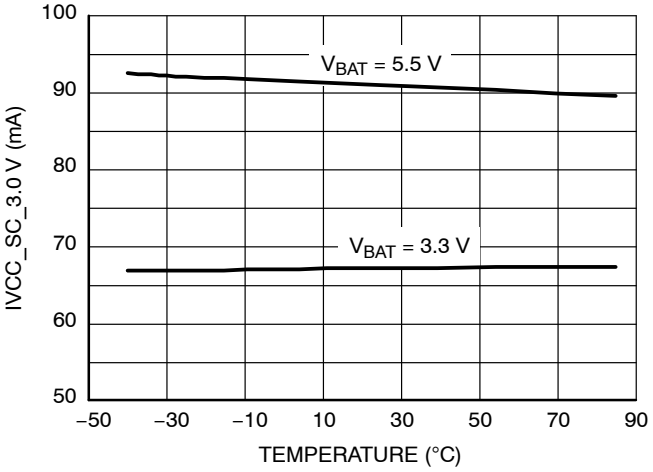


Figure 5. Short Circuit Current IV_{CC}_SC vs Temperature at SIM_V_{CC} = 3.0 V (MOD_V_{CC} = HIGH)

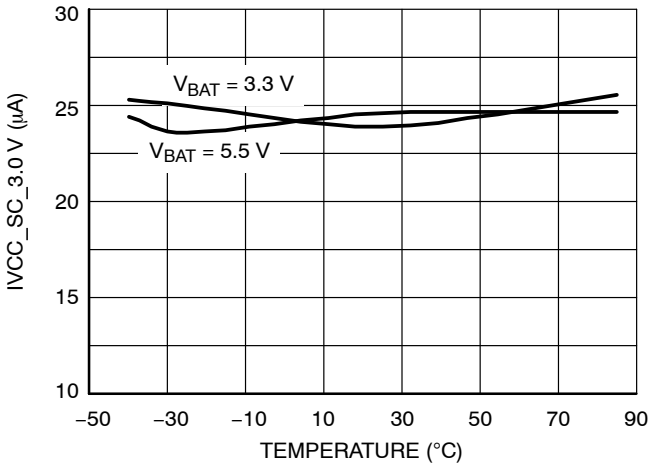


Figure 6. I_{BAT} vs temperature at 3.0 V

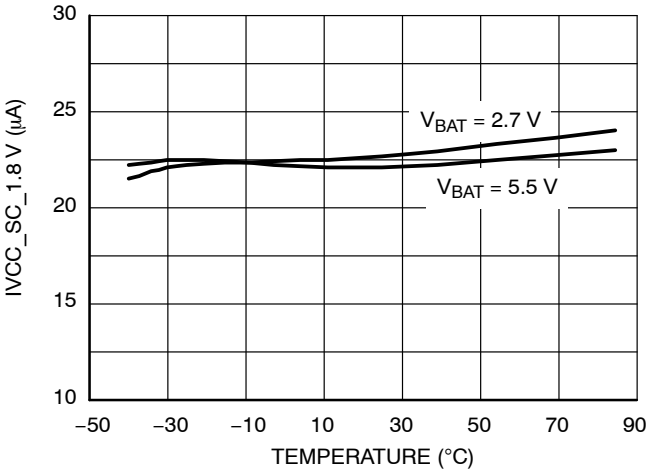


Figure 7. IV_{BAT} vs Temperature at 1.8 V

アプリケーション情報

カード電源コンバータ

NCN4555インタフェースDC−DCコンバータは、1.8 Vまたは3.0 Vで50 mAを超える電流を供給できる低ドロップアウト電圧レギュレータです。このデバイスは、標準25μA未満の超低静止電流を特長としています（Figure 6および7）。MOD_V_{CC}は、1.8 V（MOD_V_{CC} = ロー）または3.0 V（MOD_V_{CC} = ハイ）の安定化電圧を選択するロジック・レベル信号を受け入れる選択入力です。また、NCN4555にはレギュレータ出力のターン・オフまたはターン・オンを可能にするシャットダウン入力があります。シャットダウン・モードでの消費電力は一般に数10 nA程度です（30 nA標準）。Figure 8に、NCN4555電圧レギュレータの簡略図を示します。SIM_V_{CC}出力は内部で電流制限され、短絡から保護されています。短絡電流IV_{CC}は、温度によって変化せずSIM_V_{CC}です。この電流はV_{BAT}によって通常60ー90 mAの範囲で変化します（Figure 4および5）。

安定した満足のいくLDO動作を保証するために、SIM_V_{CC}出力は1.0 μFのバイパス・セラミック・コンデンサを介してグランドに接続されます。この入力で、V_{BAT}は0.1 μFのセラミック・コンデンサでグランドにバイパスされます。

レベル・シフタ

レベル・シフタは、マイクロコントローラとスマート・カード間に存在する可能性のある電圧差に対応します。RESETおよびCLOCKレベル・シフタは単方向で、両方とも同じ構成を備えています。

双方向I/Oラインは、MCUとSIMカード間の電圧差を両方向で自動的に適合させる方法を提供します。プルアップ抵抗に加えて、アクティブなプルアップ回路（Figure 8、Q1およびQ2）が浮遊容量の高速充電を提供し、立ち上がり時間が完全にISO7816仕様の範囲内になります。

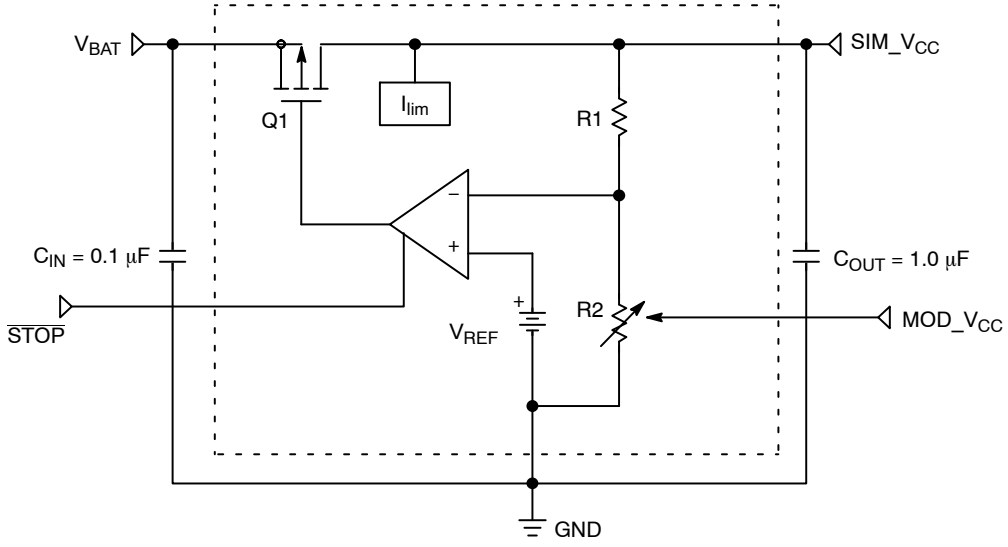


Figure 8. Simplified Block Diagram of the LDO Voltage Regulator

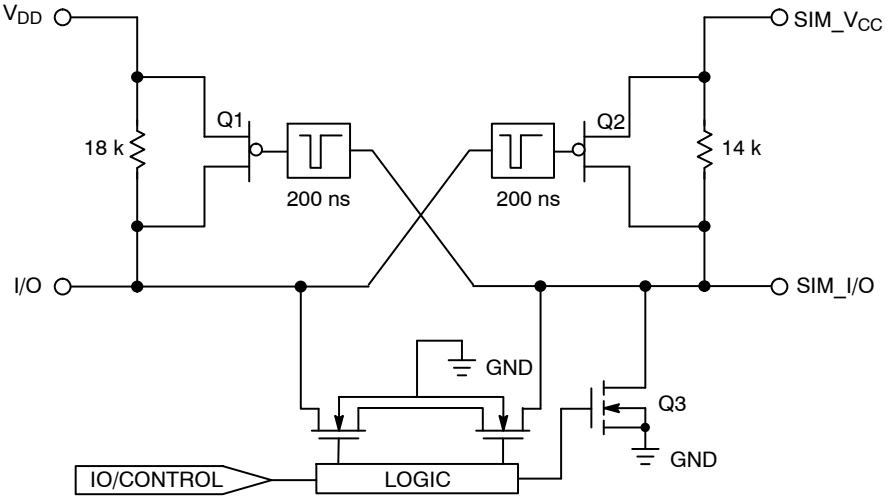


Figure 9. Basic I/O Line Interface

Figure 10に示す標準的な波形は、アクセラレータの動作を示しています。最初の200 ns（標準）の間、立ち上がり時間の傾きは浮遊容量に関連するプルアップ抵抗にのみ関係します。この期間中、PMOSデバイスは入力電圧がV_{gs}スレッショルド未満なのでアクティブになりません。Figure 10に示すとおり、入力の傾きがV_{gsth}と交差すると、反対側のワンショットがアクティブになり、低インピーダンスを提供してコンデンサを充電して、立ち上がり時間を長くします。ラインの反対側にも同じメカニズムが適用され、システムの最適化が図られます。

入力シュミット・トリガ

すべてのロジック入力ピン(I/0およびSIM_I/0を除く、Figure 3参照)に、シュミット・トリガ回路が内蔵され、NCN4555動作が無制御状態になるのを防止します。関連ピンの標準ダイナミック特性をFigure 11に記載します。

出力信号は、入力電圧が0.7 x V_{DD}を超えると確実にハイに、また出力が0.4 V未満になると確実にローになることが保証されます。

シャットダウン動作

アプリケーションに必要な電力の節減やその他の目的のために、ピン$\overline{\text{STOP}}$をローに設定して、NCN4555をシャットダウン・モードにすることができます。他方、V_{DD}が1.1 V(標準)より低くなると、デバイスは自動的にシャットダウン・モードに入ります。

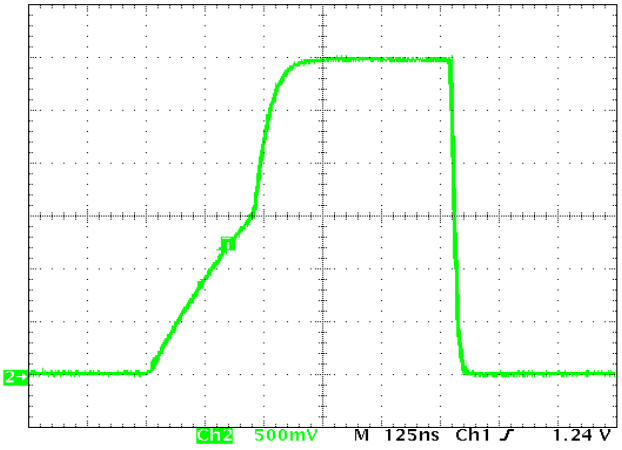


Figure 10. SIM_IO Typical Rise and Fall Times with Stray Capacitance > 30 pF (33 pF Capacitor Connected on the Board)

ESD保護回路

NCN4555 SIMインタフェースは、すべてのSIMピン(SIM_IO、SIM_CLK、SIM_RST、SIM_V_{CC}、GND)に対して7kVを超えるHBM ESD電圧保護を備えています。それ以外のすべてのピン(マイクロコントローラ側)は最小2 kVを維持します。これらの値は、回路が適切に動作するために追加された外付けコンデンサを考慮に入れないで、完全な状態のデバイスに対して保証されています。結果的に動作条件では、SIMピンで7 kVよりずっと大きな値を維持できるため、ISO7816規格(4 kV)に必要なHBM ESD電圧をはるかに超える静電気放電から完全に保護されます。

プリント基板レイアウト

モバイルまたはポータブル環境で良好かつ効率的なデバイス動作を達成し、性能を十分に活用するために、慎重なレイアウト・ルーチングが適用されます。

バイパス・コンデンサをデバイス・ピンのできるだけ近くに接続して(SIM_V_{CC}、V_{DD}、またはV_{BAT})、寄生的動作（リップルやノイズ）をできるだけ減らす必要があります。セラミック・コンデンサの使用を推奨します。

QFN−16パッケージの露出パッドをグランドと未接続ピン(NC)に接続します。比較的大きなグランド・プレーンを推奨します。

Figures 12および13に、評価環境におけるPCBデバイスの実装例を示します。

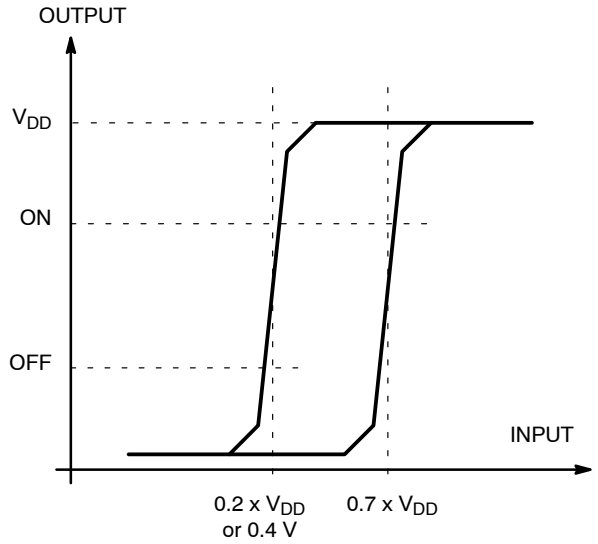


Figure 11. Typical Schmitt Trigger Characteristics

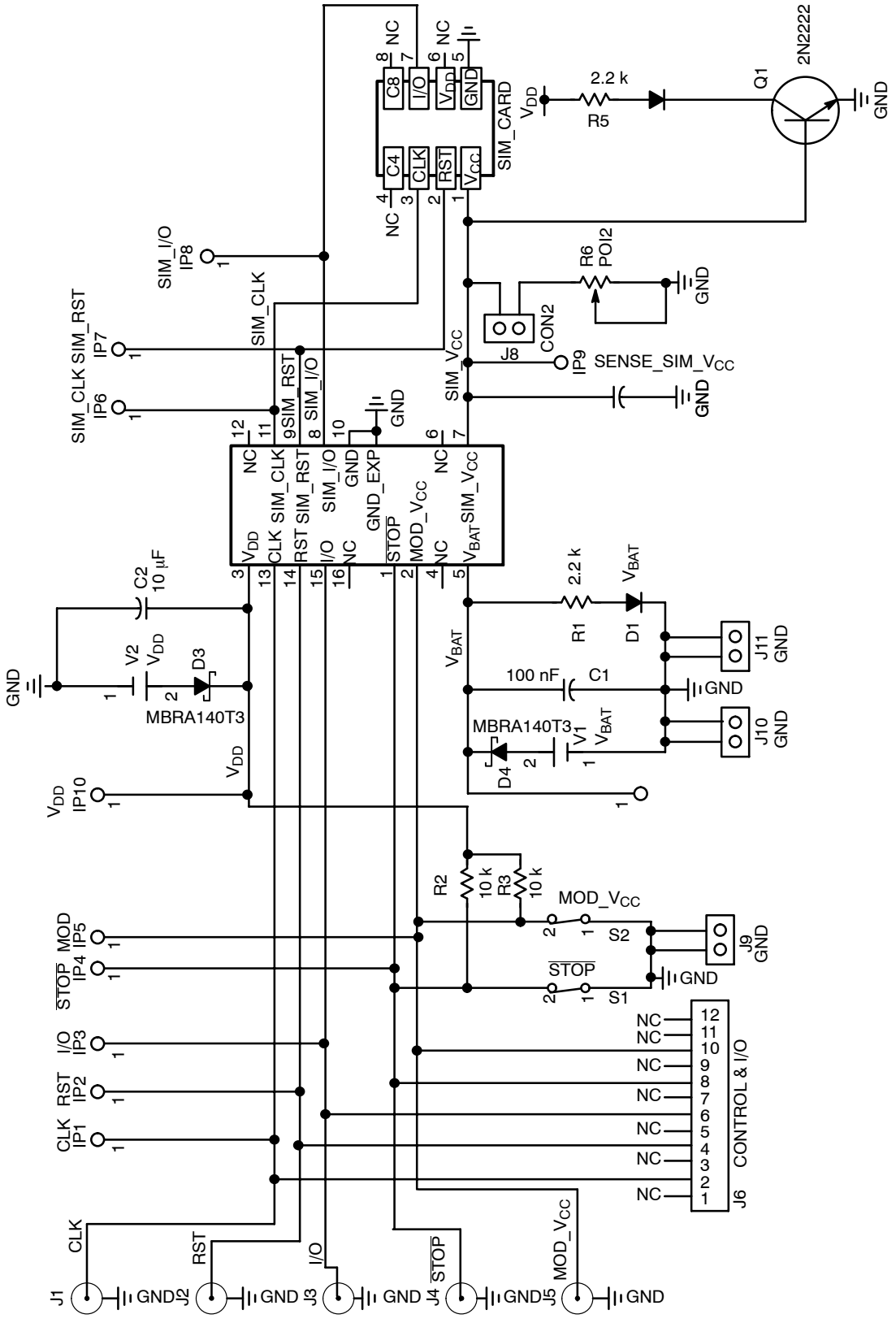
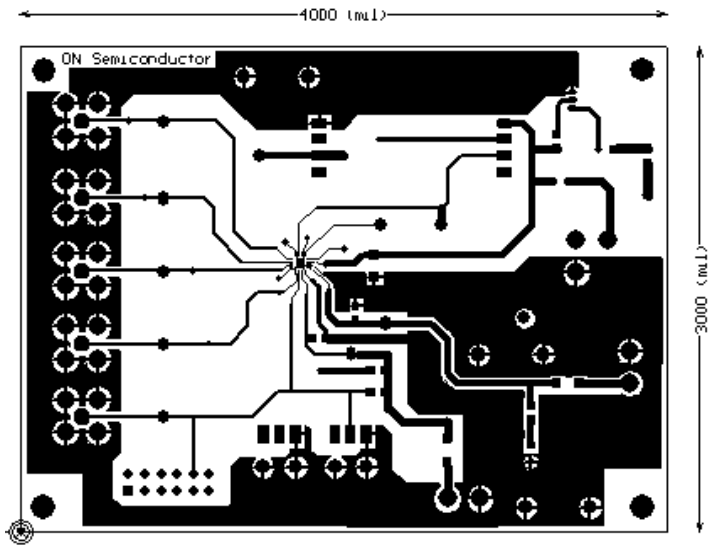
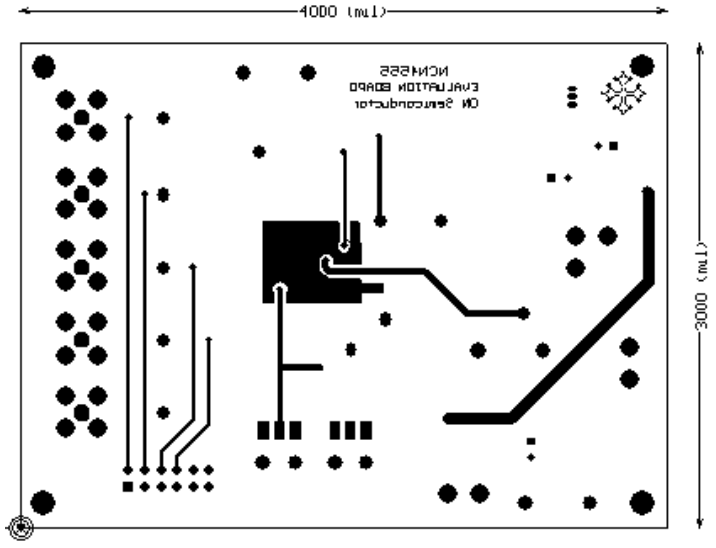


Figure 12. NCN4555 engineering test board schematic diagram



Top Layer



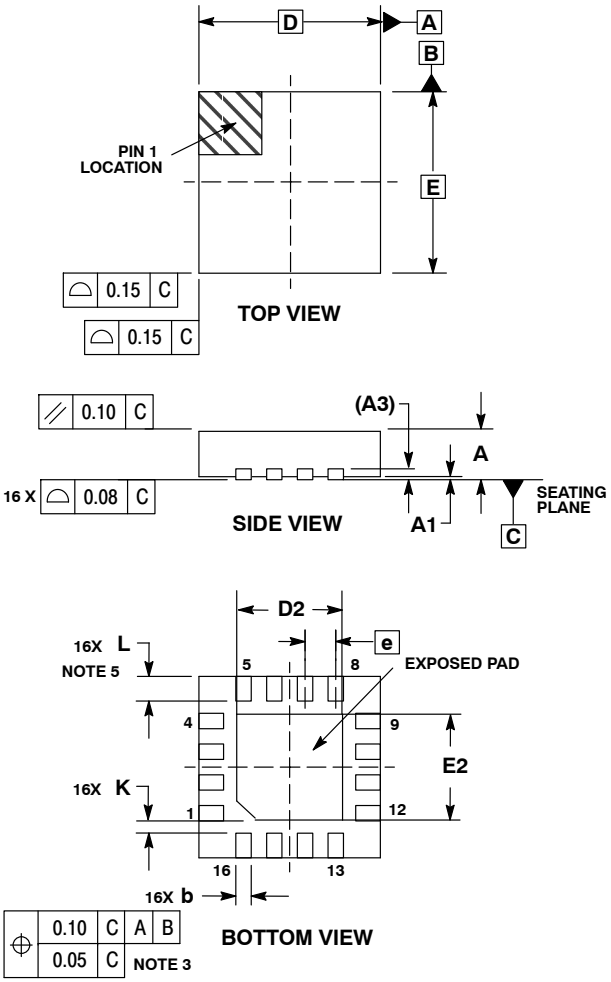
Bottom Layer

Figure 13. NCN4555 Printed Circuit Board Layout (Engineering board)

QFN16 3*3*0.75 MM, 0.5 P
CASE 488AK−01
ISSUE O

DATE 13 SEP 2004

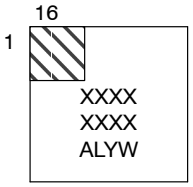
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**QFN16, 3*3*0.75 MM, 0.5 PITCH**		**PAGE 1 OF 1**

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