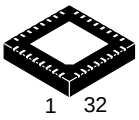
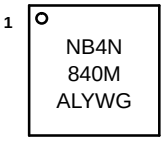
# 3.3 V 3.2 Gb/s Dual Differential Clock/Data 2 x 2 Crosspoint Switch with CML Output and Internal Termination

# NB4N840M




**QFN32**
**MN SUFFIX**
**CASE 488AM**

**MARKING DIAGRAM**




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

## Description

The NB4N840M is a high−bandwidth fully differential dual 2 x 2 crosspoint switch with CML inputs/outputs that is suitable for applications such as SDH/SONET, DWDM, Gigabit Ethernet and high speed switching. Fully differential design techniques are used to minimize jitter accumulation, crosstalk, and signal skew, which make this device ideal for loop−through and protection channel switching applications.

Internally terminated differential CML inputs accept AC−coupled LVPECL (Positive ECL) or direct coupled CML signals. By providing internal 50 Ω input and output termination resistor, the need for external components is eliminated and interface reflections are minimized. Differential 16 mA CML outputs provide matching internal 50 Ω terminations, and 400 mV output swings when externally terminated, 50 Ω to $V_{CC}$.

Single−ended LVCMOS/LVTTL SEL inputs control the routing of the signals through the crosspoint switch which makes this device configurable as 1:2 fan−out, repeater or 2 x 2 crosspoint switch. The device is housed in a low profile 5 x 5 mm 32−pin QFN package.

## Features

- Plug−in compatible to the MAX3840 and SY55859L
- Maximum Input Clock Frequency 2.7 GHz
- Maximum Input Data Frequency 3.2 Gb/s
- 225 ps Typical Propagation Delay
- 80 ps Typical Rise and Fall Times
- 7 ps Channel to Channel Skew
- 430 mW Power Consumption
- < 0.5 ps RMS Jitter
- 7 ps Peak−to−Peak Data Dependent Jitter
- Power Saving Feature with Disabled Outputs
- Operating Range: $V_{CC}$ = 3.0 V to 3.6 V with $V_{EE}$ = 0 V
- CML Output Level (400 mV Peak−to−Peak Output), Differential Output
- These are Pb−Free Devices

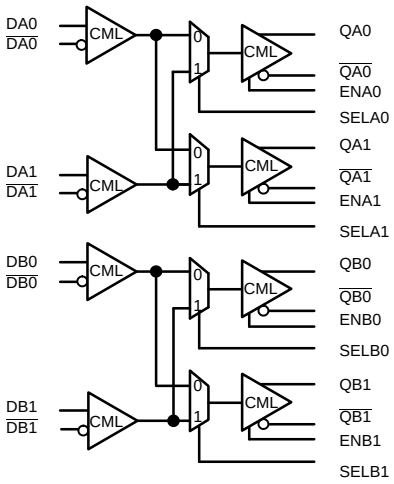



**Figure 1. Functional Block Diagram**

## ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

**Table 1. TRUTH TABLE**

| SELA0/SELB0 | SELA1/SELB1 | ENA0/ENA1 | ENB0/ENB1 | QA0/QB0 | QA1/QB1 | Function |
|---|---|---|---|---|---|---|
| L | L | H | H | DA0/DB0 | DA0/DB0 | 1:2 Fanout |
| L | H | H | H | DA0/DB0 | DA1/DB1 | Quad Repeater |
| H | L | H | H | DA1/DB1 | DA0/DB0 | Crosspoint Switch |
| H | H | H | H | DA1/DB1 | DA1/DB1 | 1:2 Fanout |
| X | X | L | L | Disable/Power Down | Disable/Power Down | No output (@ $V_{CC}$) |

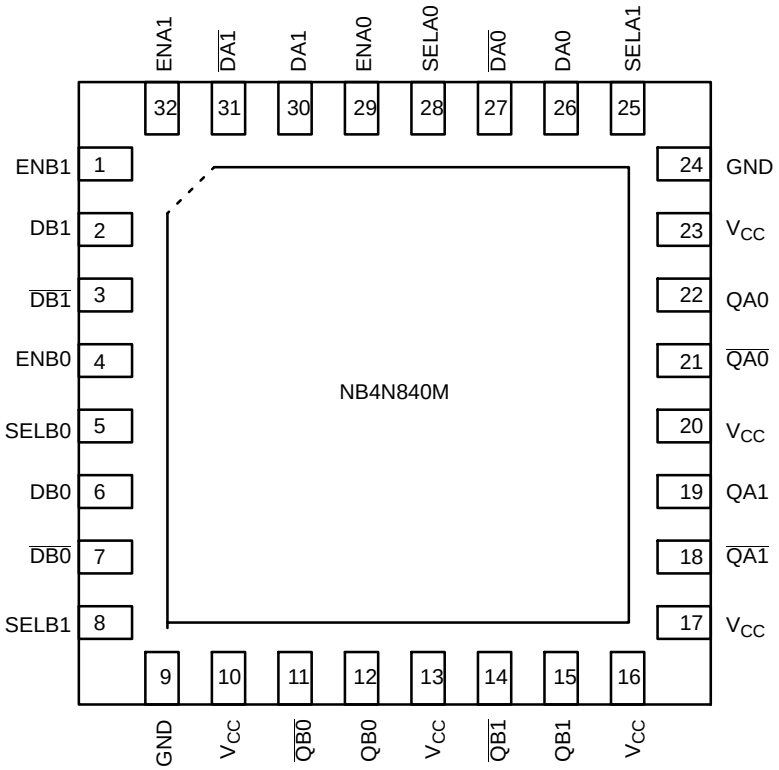



**Figure 2. Pin Configuration (Top View)**

**Table 2. PIN DESCRIPTION**

| Pin | Name | I/O | Description |
|---|---|---|---|
| 1 | ENB1 | LVTTL | Channel B1 Output Enable. LVTTL low input powers down B1 output stage. |
| 2 | DB1 | CML Input | Channel B1 Positive Signal Input |
| 3 | $\overline{DB1}$ | CML Input | Channel B1 Negative Signal Input |
| 4 | ENB0 | LVTTL | Channel B0 Output Enable. LVTTL low input powers down B0 output stage. |
| 5 | SELB0 | LVTTL | Channel B0 Output Select. See Table 1. |
| 6 | DB0 | CML Input | Channel B0 Positive Signal Input |
| 7 | $\overline{DB0}$ | CML Input | Channel B0 Negative Signal Input |
| 8 | SELB1 | LVTTL | Channel B1 Output Select. See Table 1. |
| 9,24 | GND | − | Supply Ground. All GND pins must be externally connected to power supply to guarantee proper operation. |
| 10, 13, 16, 17, 20, 23 | $V_{CC}$ | − | Positive Supply. All $V_{CC}$ pins must be externally connected to power supply to guarantee proper operation. |
| 11 | $\overline{QB0}$ | CML Output | Channel B0 Negative Output. |
| 12 | QB0 | CML Output | Channel B0 Positive Output. |
| 14 | $\overline{QB1}$ | CML Output | Channel B1 Negative Output. |
| 15 | QB1 | CML Output | Channel B1 Positive Output. |
| 18 | $\overline{QA1}$ | CML Output | Channel A1 Negative Output. |
| 19 | QA1 | CML Output | Channel A1 Positive Output. |
| 21 | $\overline{QA0}$ | CML Output | Channel A0 Negative Output. |
| 22 | QA0 | CML Output | Channel A0 Positive Output. |
| 25 | SELA1 | LVTTL | Channel A1 Output Select, LVTTL Input. See Table 1. |
| 26 | DA0 | CML Input | Channel A0 Positive Signal Input. |
| 27 | $\overline{DA0}$ | CML Input | Channel A0 Negative Signal Input. |
| 28 | SELA0 | LVTTL | Channel A0 Output Select, LVTTL Input. See Table 1. |
| 29 | ENA0 | LVTTL | Channel A0 Output Enable. LVTTL low input powers down A0 output stage. |
| 30 | DA1 | CML Input | Channel A1 Positive Signal Input. |
| 31 | $\overline{DA1}$ | CML Input | Channel A1 Negative Signal Input. |
| 32 | ENA1 | LVTTL | Channel A1 Output Enable. LVTTL low input powers down A1 output stage. |
| − | EP | GND | Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat−sinking conduit. The exposed pad must be soldered to the circuit board GND for proper electrical and thermal operation. |

**Table 3. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| ESD Protection | Human Body Model<br>Machine Model | > 2000 V<br>> 110 V |
| Moisture Sensitivity (Note 1) | QFN−32 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 380 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, refer to Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | GND = 0 V | | 3.8 | V |
| $V_I$ | Positive Input | GND = 0 V | GND = $V_I$ = $V_{CC}$ | 3.8 | V |
| $V_{INPP}$ | Differential Input Voltage \|D − $\overline{D}$\| | | | 3.8 | V |
| $I_{IN}$ | Input Current Through Internal 50 Ω Resistor | Static<br>Surge | | 45<br>80 | mA<br>mA |
| $I_{OUT}$ | Output Current | Continuous<br>Surge | | 25<br>80 | mA<br>mA |
| $T_A$ | Operating Temperature Range | QFN−32 | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 2) | 0 lfpm<br>500 lfpm | QFN−32<br>QFN−32 | 31<br>27 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 2S2P (Note 3) | QFN−32 | 12 | °C/W |
| $T_{sol}$ | Wave Solder Pb−Free | <3 sec @ 260 C | | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 5. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS** $V_{CC}$ = 3.0 V to 3.6 V, $T_A$ = −40°C to +85°C

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current (All outputs enabled) | | 130 | 170 | mA |
| $Vout_{diff}$ | CML Differential Output Swing (Note 4, Figures 5 and 12) | 640 | 800 | 1000 | mV |
| $V_{CMR}$ (Note 6) | CML Output Common Mode Voltage (Loaded 50 Ω to $V_{CC}$) | | $V_{CC}$ − 200 | | mV |
| | CML Single−Ended Input Voltage Range | $V_{CC}$ − 800 | | $V_{CC}$ + 400 | mV |
| $V_{ID}$ | Differential Input Voltage ($V_{IHD}$ − $V_{ILD}$) | 300 | | 1600 | mV |
| **LVTTL CONTROL INPUT PINS** | | | | | |
| $V_{IH}$ | Input HIGH Voltage (LVTTL Inputs) | 2000 | | | mV |
| $V_{IL}$ | Input LOW Voltage (LVTTL Inputs) | | | 800 | mV |
| $I_{IH}$ | Input HIGH Current (LVTTL Inputs) | −10 | | 10 | μA |
| $I_{IL}$ | Input LOW Current (LVTTL Inputs) | −10 | | 10 | μA |
| $R_{TIN}$ | CML Single−Ended Input Resistance | 42.5 | 50 | 57.5 | Ω |
| $R_{TOUT}$ | Differential Output Resistance | 85 | 100 | 115 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. CML outputs require 50 Ω receiver termination resistors to $V_{CC}$ for proper operation (Figure 10).
5. Input and output parameters vary 1:1 with $V_{CC}$.
6. $V_{CMR}$ min varies 1:1 with $V_{EE}$, $V_{CMR}$ max varies 1:1 with $V_{CC}$.

**Table 6. AC CHARACTERISTICS** $V_{CC}$ = 3.0 V to 3.6 V, $V_{EE}$ = 0 V (Note 7, Figure 9)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $V_{OUTPP}$ | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \le 2$ GHz<br>(See Figure 3) $f_{in} \le 3$ GHz<br>$f_{in} \le 3.5$ GHz | 280<br>235<br>170 | 365<br>310<br>220 | | 280<br>235<br>170 | 365<br>310<br>220 | | 280<br>235<br>170 | 365<br>310<br>220 | | mV |
| $f_{DATA}$ | Maximum Operating Data Rate | 3.2 | | | 3.2 | | | 3.2 | | | Gb/s |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay to Output Differential D/$\overline{D}$ to Q/$\overline{Q}$ | 140 | 225 | 340 | 140 | 225 | 340 | 140 | 225 | 340 | ps |
| $t_{SKEW}$ | Duty Cycle Skew (Note 8)<br>Within−Device Skew (Figure 4)<br>Device−to−Device Skew (Note 12) | | 5<br>5<br>20 | 25<br>25<br>85 | | 5<br>5<br>20 | 25<br>25<br>85 | | 5<br>5<br>20 | 25<br>25<br>85 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter (Note 10) $f_{in} \le 3.2$ GHz<br>Peak−to−Peak Data Dependent Jitter $f_{in}$ = 2.5 Gb/s<br>(Note 11) $f_{in}$ = 3.2 Gb/s | | 0.15<br>7<br>7 | 0.5<br>20<br>20 | | 0.15<br>7<br>7 | 0.5<br>20<br>20 | | 0.15<br>7<br>7 | 0.5<br>20<br>20 | ps |
| | Crosstalk−Induced RMS Jitter (Note 13) | | | 0.5 | | | 0.5 | | | 0.5 | ps |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 9) | 150 | | 800 | 150 | | 800 | 150 | | 800 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times @ 0.5 GHz Q, $\overline{Q}$<br>(20% − 80%) | | 80 | 135 | | 80 | 135 | | 80 | 135 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7. Measured by forcing $V_{INPP}$ (MIN) from a 50% duty cycle clock source. All loading with an external $R_L$ = 50 Ω to $V_{CC}$. Input edge rates 40 ps (20% − 80%).
8. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 0.5 GHz.
9. $V_{INPP}$ (MAX) cannot exceed 800 mV. Input voltage swing is a single−ended measurement operating in differential mode.
10. Additive RMS jitter using 50% duty cycle clock input signal.
11. Additive peak−to−peak data dependent jitter using input data pattern with PRBS $2^{23}$−1 and K28.5, $V_{INPP}$ = 400 mV.
12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
13. Data taken on the same device under identical condition.

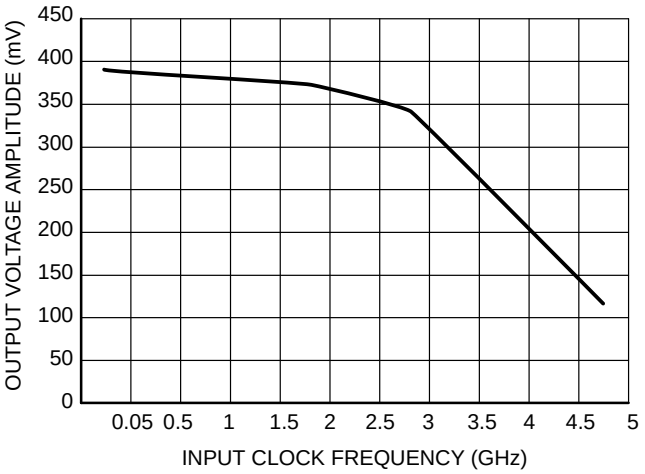



**Figure 3. Output Voltage Amplitude ($V_{OUTPP}$) vs. Input Clock Frequency ($f_{IN}$) at Ambient Temperature (Typ)**

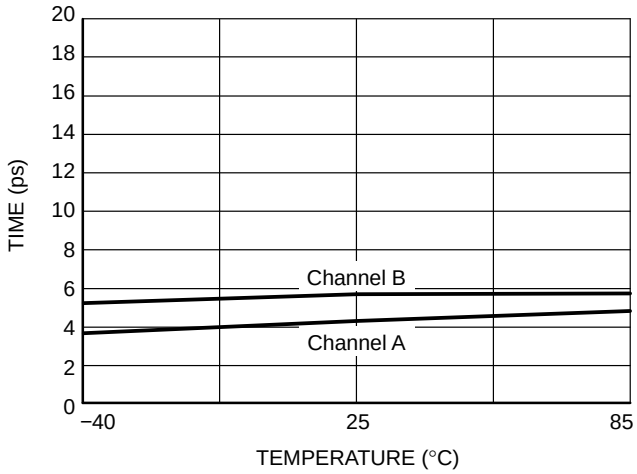



**Figure 4. Within−Device Skew vs. Temperature at $V_{CC}$ = 3.3 V**

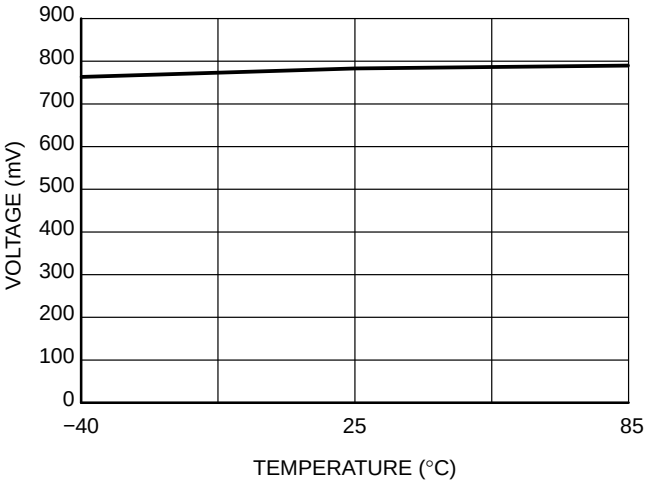



**Figure 5. CML Differential Voltage vs. Temperature**

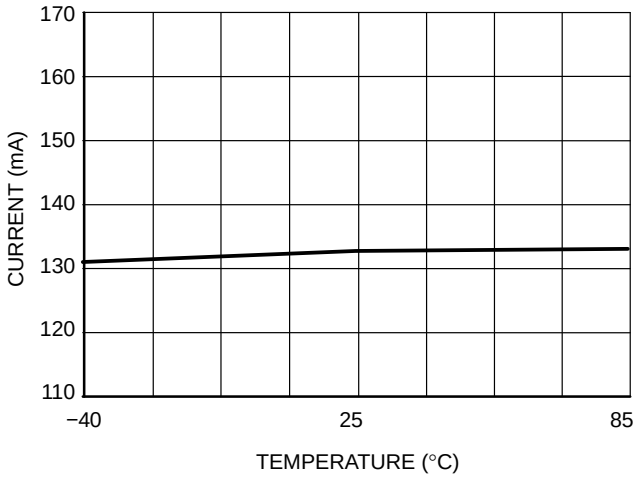



**Figure 6. Supply Current vs. Temperature (All 4 Outputs Enabled)**

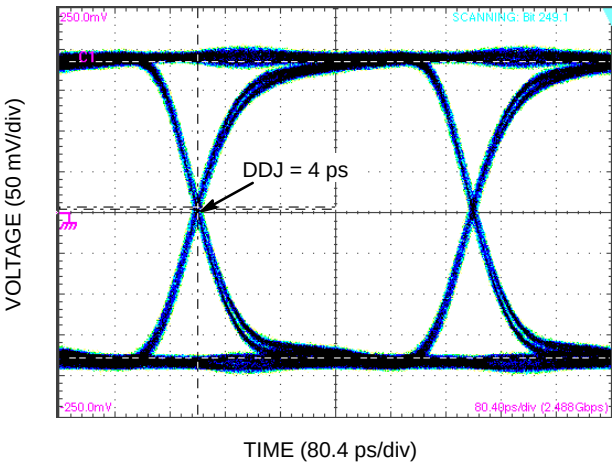



**Figure 7. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}$–1 (Input Signal DDJ = 12 ps)**

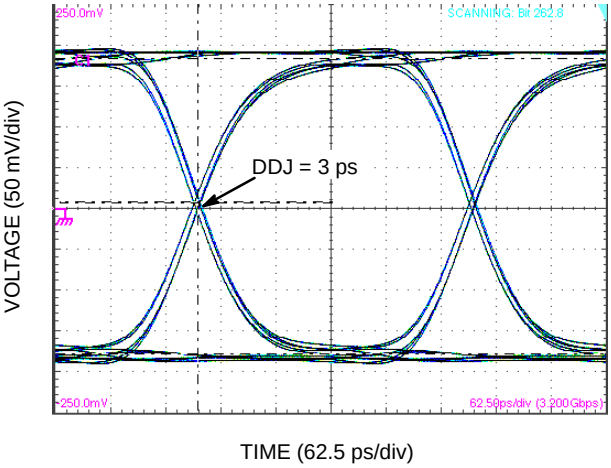



**Figure 8. Typical Output Waveform at 3.2 Gb/s with K28.5 (Input Signal DDJ = 14 ps)**

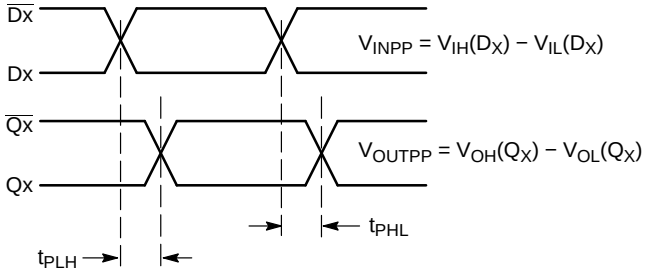



**Figure 9. AC Reference Measurement**

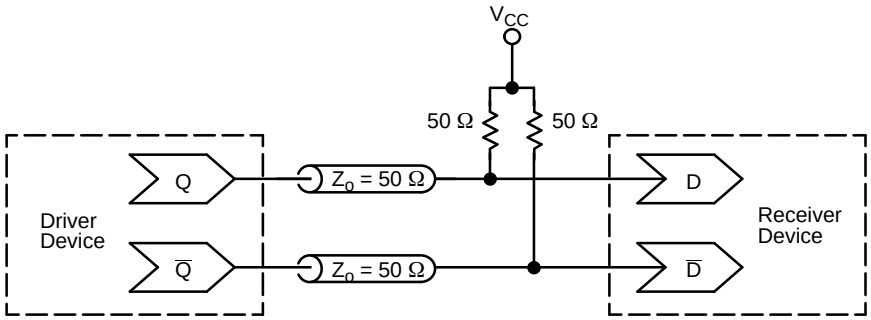



**Figure 10. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8173/D)**

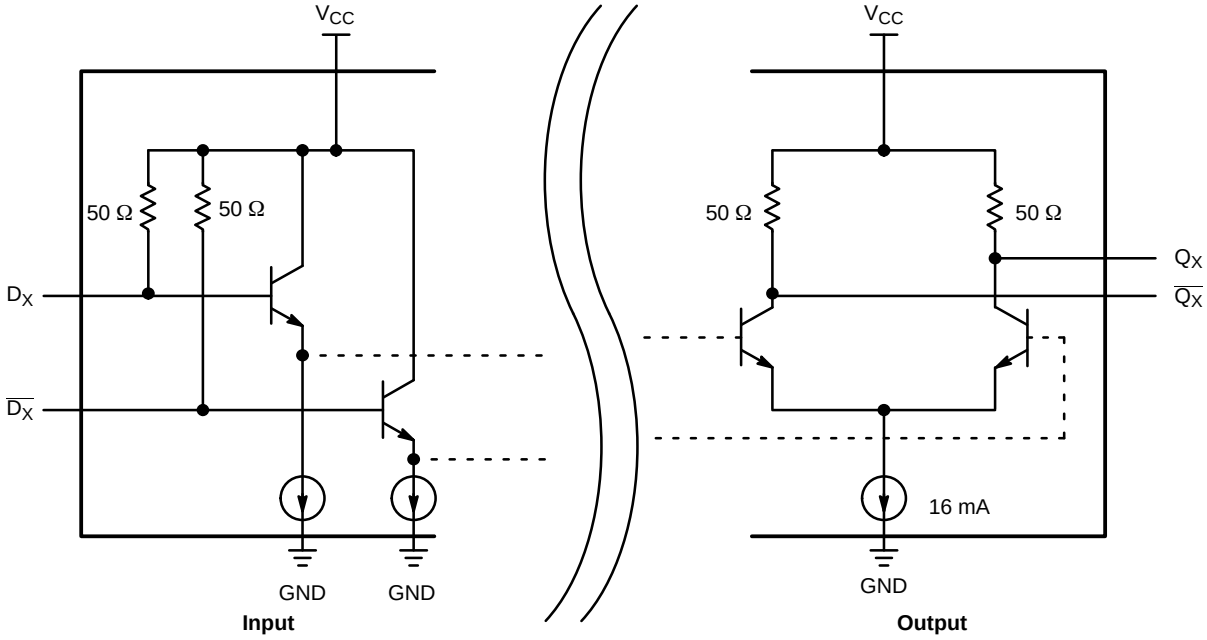



**Figure 11. CML Input and Output Structure**

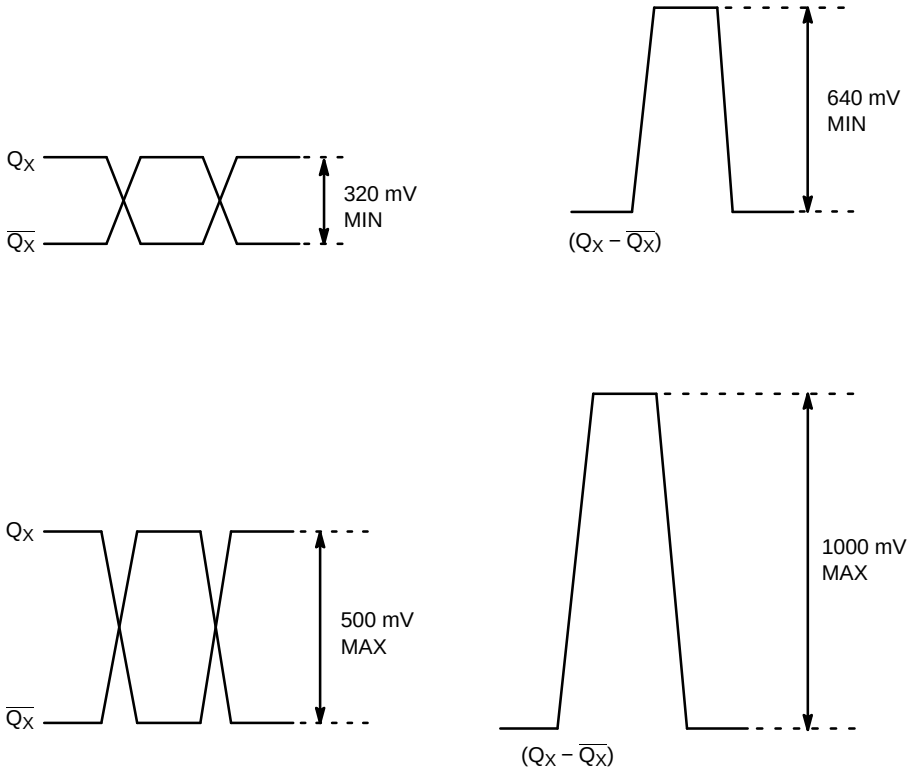



**Figure 12. CML Output Levels**

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| NB4N840MMNG | QFN32<br>(Pb−Free) | 74 Units / Rail |
| NB4N840MMNR4G | QFN32<br>(Pb−Free) | 1000 / Tape & Reel |

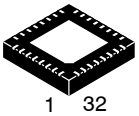
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

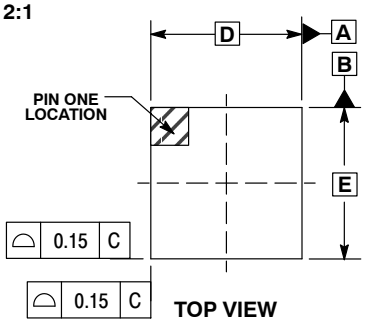
ON Semiconductor®

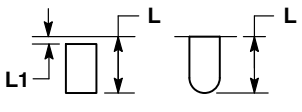
**QFN32 5x5, 0.5P**
CASE 488AM
ISSUE A

DATE 23 OCT 2013

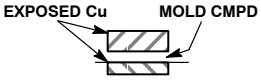



**SCALE 2:1**

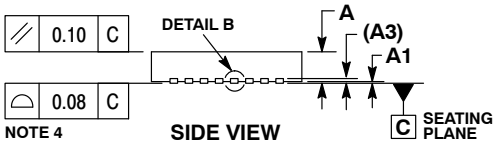


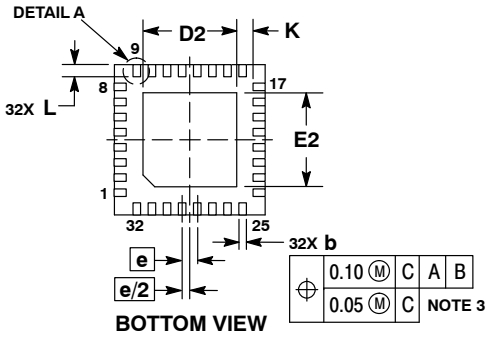




**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**




**DETAIL B**
**ALTERNATE CONSTRUCTION**

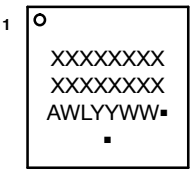



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 5.00 BSC | |
| D2 | 2.95 | 3.25 |
| E | 5.00 BSC | |
| E2 | 2.95 | 3.25 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

### GENERIC MARKING DIAGRAM*

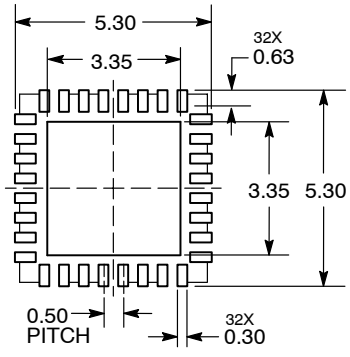



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON20032D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **QFN32 5x5 0.5P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales