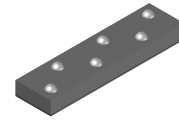# Actuator Control Driver with Hall Sensor

Advance Information
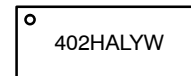# LC898402XHTBG

WLCSP6, 0.58 x 2.19 x 0.265
Case 567XY

Overview

This LSI is the actuator driver with integrated Hall and constant current driver. It has also a built−in EEPROM and temperature sensor. It can realize high−performance feedback control with external PID controller.

Features

- Built-in Digital Operation Circuit
  - Any Coefficient can be Specified by 2-wire Serial I/F (TWIF)
- 2-wire Serial Interface
  - I^2C−compatible Protocol Mode
  - High−speed Protocol Mode
  - 16 Selectable Slave Addresses
    - 50h(W) / 51h(R)
    - 74h(W) / 75h(R)
    - E8h(W) / E9h(R)
    - E4h(W) / E5h(R) factory−configured
    - Other 12 Addresses can be selected
- Built-in A/D Converter
- Built-in D/A Converter
  - Hall Offset
  - Constant Current Bias
- Built-in Hall Sensor
  - Si Hall Sensor
- Built-in VGA
  - Hall Amplifier
- Built-in EEPROM
  - 64 byte (16 byte/page)
- Built-in OSC
- Built-in Bi-Direction Constant Current Driver
  - 130 mA
- Package
  - WLCSP 6-pin (2×3 pin), Thickness Max 0.29 mm, with Backside Coat
  - Pb-Free, Halogen Free/BFR Free and RoHS Compliant
- Supply Voltage
  - V_{DD} (2.6 V to 3.3 V)

MARKING DIAGRAM

402HALYW

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping[†]
LC898402XHTBG	WLCSP6 (Pb−Free / Halogen Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN DESCRIPTION

PIN DESCRIPTION

Type	
I	INPUT
O	OUTPUT
B	BIDIRECTION
P	Power Supply, GND
NC	NOT CONNECT

- 2-wire Serial Interface
  - SCL   B   2-wire Serial Interface Clock Pin
  - SDA   B   2-wire Serial Interface Data Pin
- Driver Interface
  - OUT1   O   Driver Output (to Actuator)
  - OUT2   O   Driver Output (to Actuator)
- Power Supply Pin
  - VDD   P   Power Supply
  - VSS   P   GND

Process When Pins are Not Used:
PIN TYPE "O" – Ensure that it is set to OPEN.
PIN TYPE "I" – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused.
                        (Please contact **onsemi** for more information about selection of VDD or VSS.)
PIN TYPE "B" – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

LC898402XHTBG

PIN LAYOUT

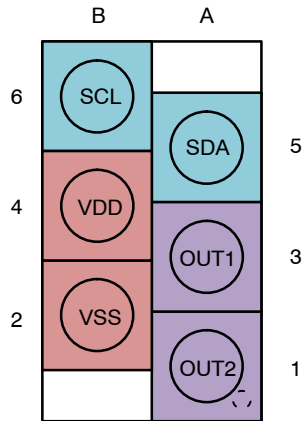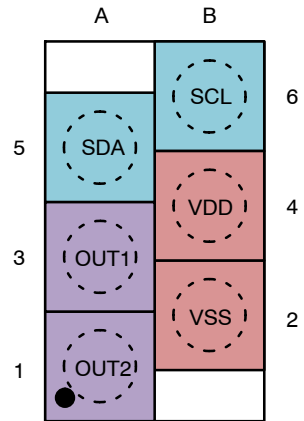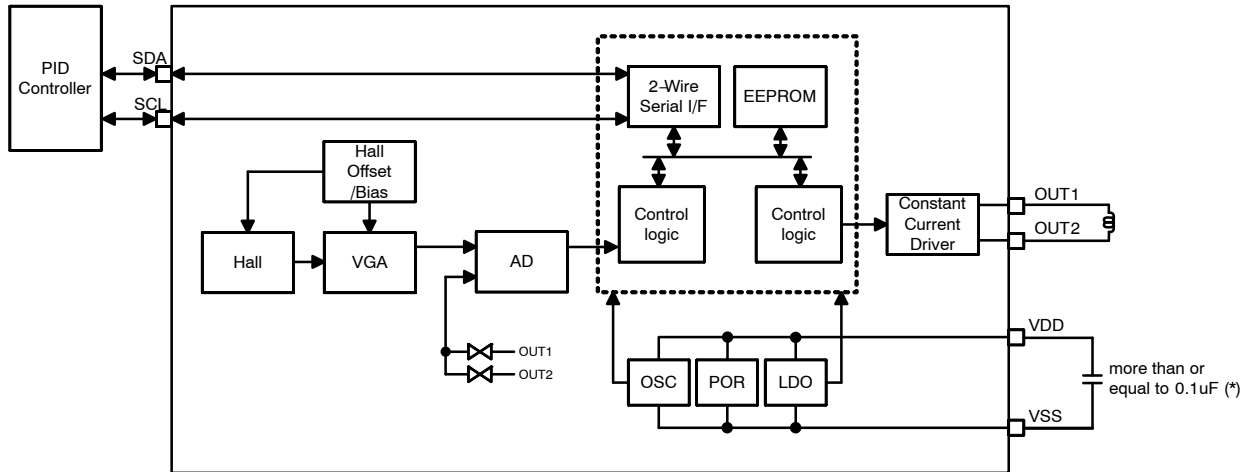| Circuit Name	Number of PINs
Driver	2
Power	2
Logic	2

Figure 1. Bottom View
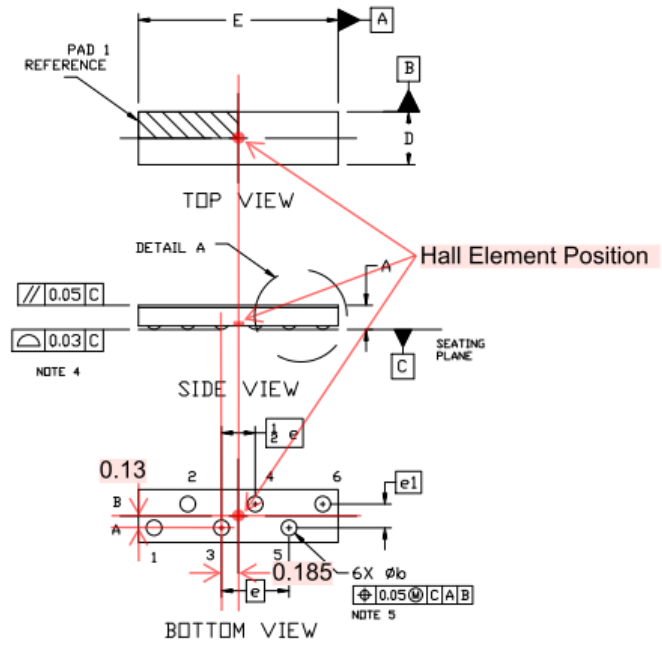

Figure 2. Top View

BLOCK DIAGRAM

*Consider capacitance of capacitor between VDD and VSS. According to power source environment, attach an additional capacitor in camera module.

Figure 3. Block Diagram

HALL ELEMENT POSITION

Please refer to package diagram for each dimension.

ELECTRICAL CHARACTERISTICS

Table 1. ABSOLUTE MAXIMUM RATINGS (VSS = 0 V)

Symbol	Parameter	Condition	Value	Unit
$V_{DD}33$ max	Supply Voltage	$T_A \leq 25°C$	−0.3 to 4.6	V
V_I33, V_O33	Input/Output Voltage	$T_A \leq 25°C$	−0.3 to $V_{DD}33$+0.3	V
T_{stg}	Storage Ambient Temperature		−55 to +125	°C
T_{opr}	Operating Ambient Temperature		−30 to +70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS (T_A = −30 to +70°C, VSS = 0 V)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{DD}33$	Supply Voltage	2.6	2.8	3.3	V
V_{IN}	Input Voltage Range	0		$V_{DD}33$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. DC CHARACTERISTICS: INPUT/OUTPUT LEVEL (VSS = 0 V, VDD = 2.6 V to 3.3 V, T_A = −30 to +70°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit	Applicable Pins
VIH	High-level Input Voltage	CMOS Compliant Schmitt	1.4			V	SCL, SDA
VIL	Low-level Input Voltage				0.4	V	
VOL	Low-level Output Voltage	IOL = 2 mA			0.2	V	SCL, SDA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. DRIVER OUTPUT (OUT1, OUT2) (VSS = 0 V, VDD = 2.8 V, T_A = 25°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit	Applicable Pins
I_{full}	Maximum Current		123.5	130	136.5	mA	OUT1, OUT2

Table 5. NON-VOLATILE MEMORY CHARACTERISTICS

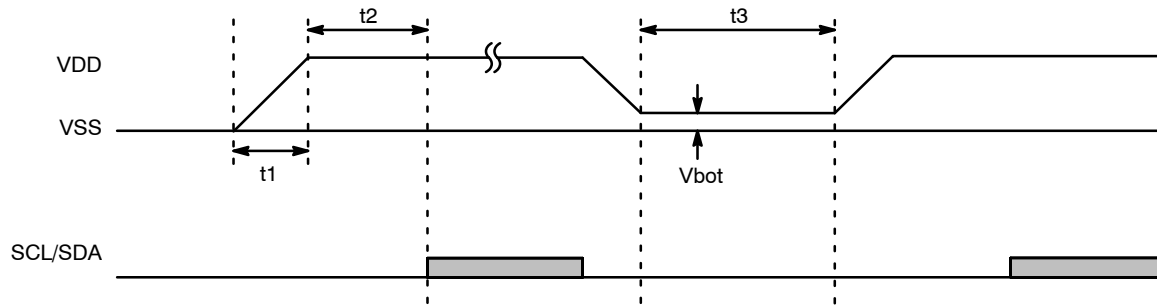| Symbol	Characteristic	Condition	Min	Typ	Max	Unit	Applicable Circuit
EN	Endurance				1000	Cycles	EEPROM
RT	Data Retention		10			Years	
t_{WT}	Write Time				20	ms	

AC CHARACTERISTICS

VDD Supply Timing

Figure 4. VDD Supply Timing

It is available to use 2-wire serial interface 5 ms later for Power On Reset of VDD.

Table 6. VDD SUPPLY TIMING

Symbol	Item	Min	Typ	Max	Unit
t1	VDD Turn On Time			3	ms
t2	2-wire Serial Interface Start Time from VDD On	5			ms
t3	VDD Off Time	100			ms
Vbot	Bottom Voltage			0.1	V

AC Specification

(a) 2−wire Serial Interface: Fast−mode and Fast−mode Plus

Figure 5 shows interface timing definition and Table 7 shows electric characteristics.
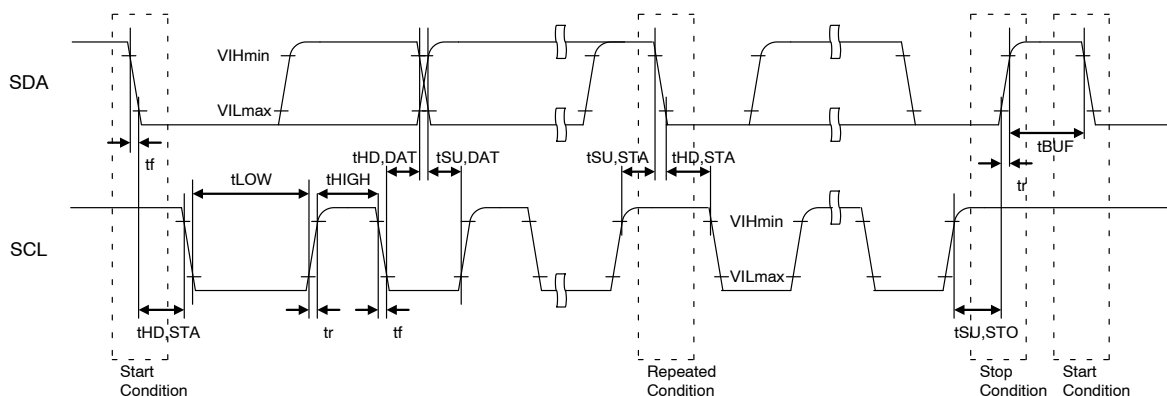
Figure 5. Fast−mode and Fast−mode Plus Timing Definition

Table 7. FAST−MODE AND FAST−MODE PLUS AC CHARACTERISTICS

Symbol	Item	Pin Name	Fast-mode			Fast-mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
FSCL	SCL Clock Frequency	SCL			400			1000	kHz
tHD,STA	START Condition Hold Time	SCL SDA	0.6			0.26			µs
tLOW	SCL Clock Low Period	SCL	1.3			0.5			µs
tHIGH	SCL Clock High Period	SCL	0.6			0.26			µs
tSU,STA	Setup Time for Repetition START Condition	SCL SDA	0.6			0.26			µs
tHD,DAT	Data Hold Time	SCL SDA	0 (Note 1)		0.9	0 (Note 1)			µs
tSU,DAT	Data Setup Time	SCL SDA	100			50			ns
tr	SDA, SCL Rising Time	SCL SDA			300			120	ns
tf	SDA, SCL Falling Time	SCL SDA			300			120	ns
tSU,STO	STOP Condition Setup Time	SCL SDA	0.6			0.26			µs
tBUF	Bus Free Time between STOP and START	SCL SDA	1.3			0.5			µs

1. This LSI is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

(b) 2−wire Serial Interface: High−speed Mode

Figure 6 shows interface timing definition and Table 8 shows electric characteristics.
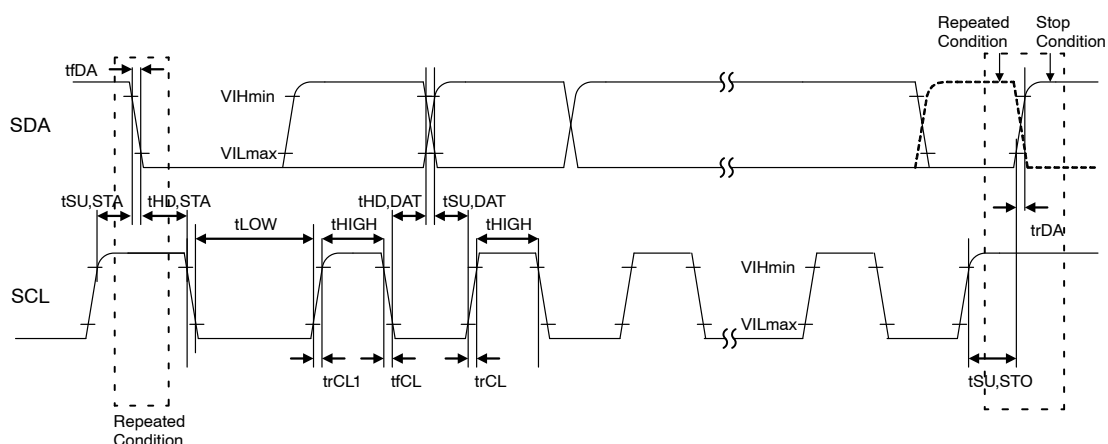
Figure 6. High−speed Mode Timing Definition
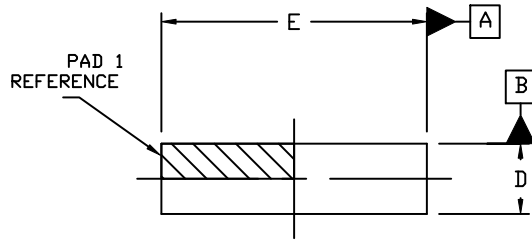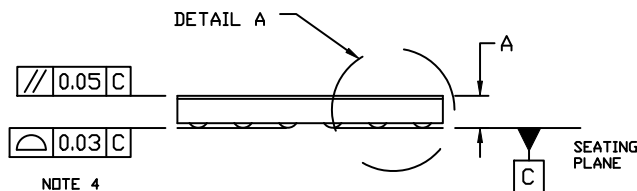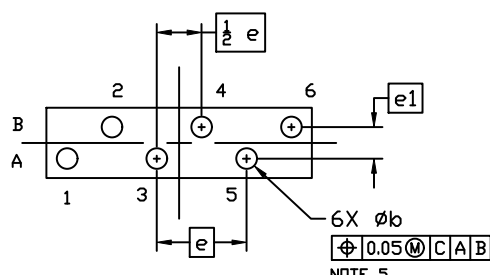
Table 8. HIGH−SPEED MODE AC CHARACTERISTICS

Symbol	Item	Pin Name	Cb = 100 pF (max)			Cb = 400 pF			Unit
			Min	Typ	Max	Min	Typ	Max	
FSCL	SCL Clock Frequency	SCL			3.4			1.7	MHz
tSU,STA	Setup Time for Repeated START Condition	SCL SDA	160			160			ns
tHD,STA	(Repeated) START Condition Hold Time	SCL SDA	160			160			ns
tLOW	SCL Clock Low Period	SCL	160			320			ns
tHIGH	SCL Clock High Period	SCL	60			120			ns
tHD,DAT	Data Hold Time	SCL SDA	0 (Note 2)		70	0 (Note 2)		150	ns
tSU,DAT	Data Setup Time	SCL SDA	10			10			ns
trCL	SCL Rising Time	SCL	10		40	20		80	ns
trCL1	SCL Rising Time After a Repeated START Condition and After an Acknowledge Bit	SCL	10		80	20		160	ns
tfCL	SCL Falling Time	SCL	10		40	20		80	ns
trDA	SDA Rising Time	SDA	10		80	20		160	ns
tfDA	SDA Falling Time	SDA	10		80	20		160	ns
tSU,STO	STOP Condition Setup Time	SCL SDA	160			160			ns
Cb	Capacitive Load for Each Bus Line	SCL and SDA lines			100			400	pF

2. This LSI is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

LC898402XHTBG

PACKAGE DIMENSIONS

WLCSP6, 0.58x2.19x0.265
CASE 567XY
ISSUE C

TOP VIEW

PAD 1 REFERENCE

E

A

B

D

SIDE VIEW

DETAIL A

// 0.05 C

⌒ 0.03 C

NOTE 4

A

C

SEATING PLANE

BOTTOM VIEW

½ e

2   4   6

B

A

1   3   5

e

e1

6X Øb

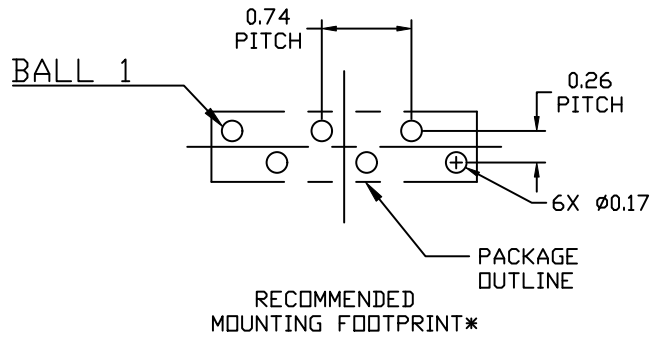⊕ 0.05 Ⓜ C A B

NOTE 5

DETAIL A

BACKSIDE COATING

A3

A2

A1
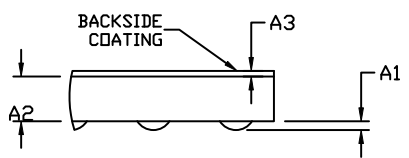
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

2. CONTROLLING DIMENSION: MILLIMETERS.

3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.

4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.24	0.265	0.29
A1	0.04 REF		
A2	0.20 REF		
A3	0.025 REF		
b	0.12	0.17	0.22
D	0.53	0.58	0.63
E	2.14	2.19	2.24
e	0.74 BSC		
e1	0.26 BSC		

BALL 1

0.74 PITCH

0.26 PITCH

6X Ø0.17

PACKAGE OUTLINE

RECOMMENDED MOUNTING FOOTPRINT*

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LC898402XHTBG

PUBLICATION ORDERING INFORMATION

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