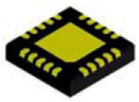
Automotive USB Power Delivery Source Controller for USB-C™

FUSB3317



QFNW20 4x4, 0.5P
CASE 484AT

FUSB3317 is a highly integrated USB Power Delivery (PD) power Source controller for USB−C that implements all functionality of USB Power Delivery 3.1 (PD) and Type−C™ 2.0 including Programmable Power Supplies (PPS). The FUSB3317 directly interfaces with a DC−DC regulator saving the cost of a load switch FET.

FUSB3317 supports various protections, adaptive Under Voltage Protection (UVP), adaptive Over Voltage Protection (OVP), Over Current Protection (OCP), CC1 and CC2 Over Voltage Protection (CC_OVP), D+ and D− Over Voltage Protection (D_OVP), VCONN Over Current Protection (VCONN_OCP), and internal and external Over Temperature protection (I_TOP and E_OTP).

Features

- PD 3.1 v1.0 and Type−C 2.0 Compliant
- Constant Voltage (CV) and Constant Current Limit (CL) Regulation
- Small Current Sensing Resistor (5 mΩ) for High Efficiency
- Directly Off Automotive Battery 4 V to 45 V Operation, Iq < 100 μA
- CC1/CC2/D+/D− Pin Protection Up to 27 V
- Automatically Scales Power Based on VBAT & NTC Temperature
- Resistor Divider or Battery Charging (BC1.2) CDP Mode
- Internal VDD and VCONN Generation
- Adaptive UVP, Adaptive OVP, I_OTP, E_OTP, CC_OVP, D_OVP and VCONN_OCP Fault Detection
- 20−pin 4 mm x 4 mm QFNW (Wettable Flanks) Package
- This is a Pb−Free Device

Typical Applications

- Power Delivery Source Controller
- DC−DC Controller Interface to USB−C Connector

End Products

- Automotive USB−C Charging Only Port
- Automotive USB−C Data and Charging Port
- Mobile and Computing Multi−Port Adapters
- Industrial Charging USB PD Ports

MARKING DIAGRAM

FUSB3317V6A = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

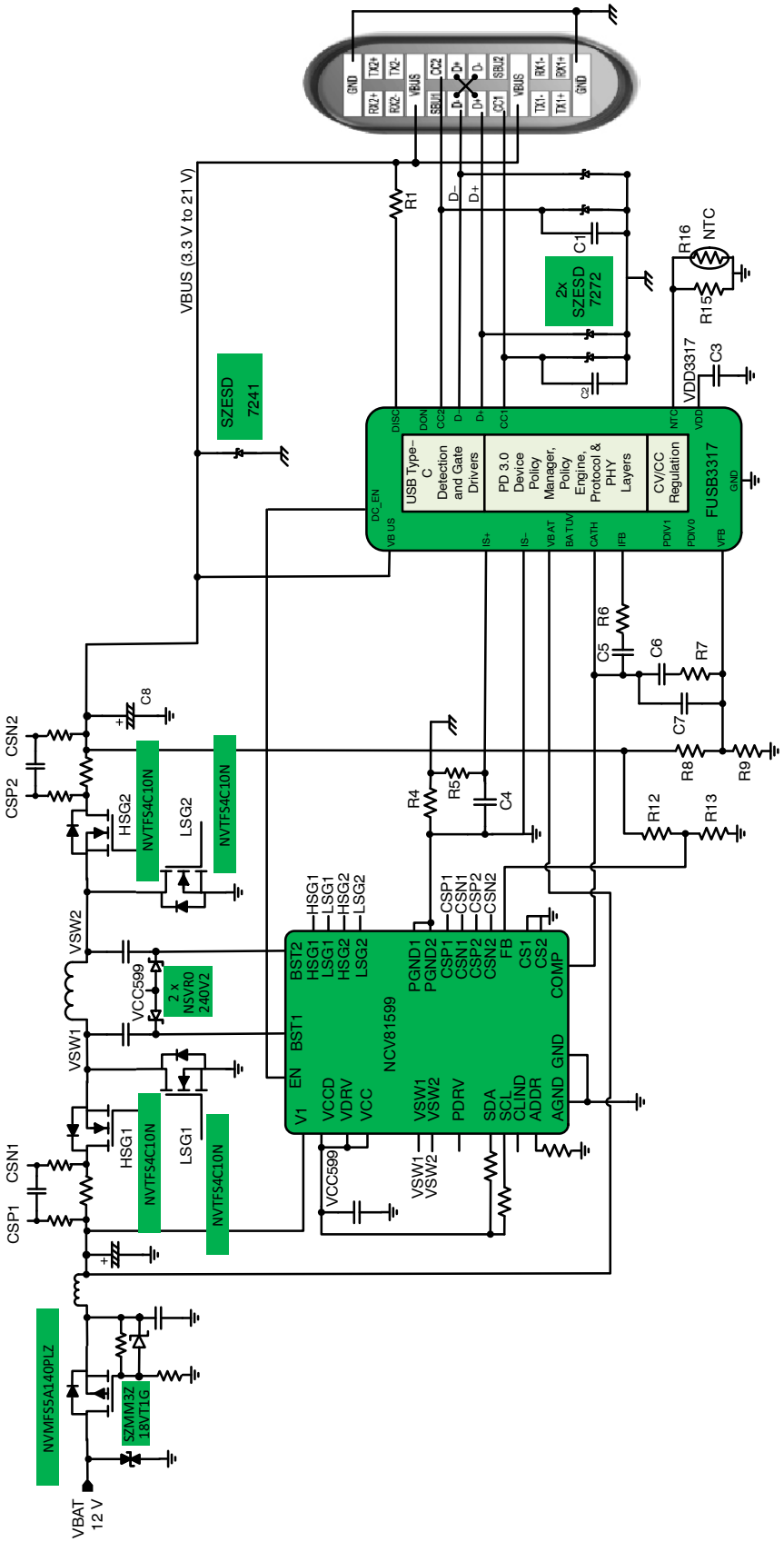


Figure 1. Application Schematic – Automotive DC/DC Reference Design Example

Block Diagram

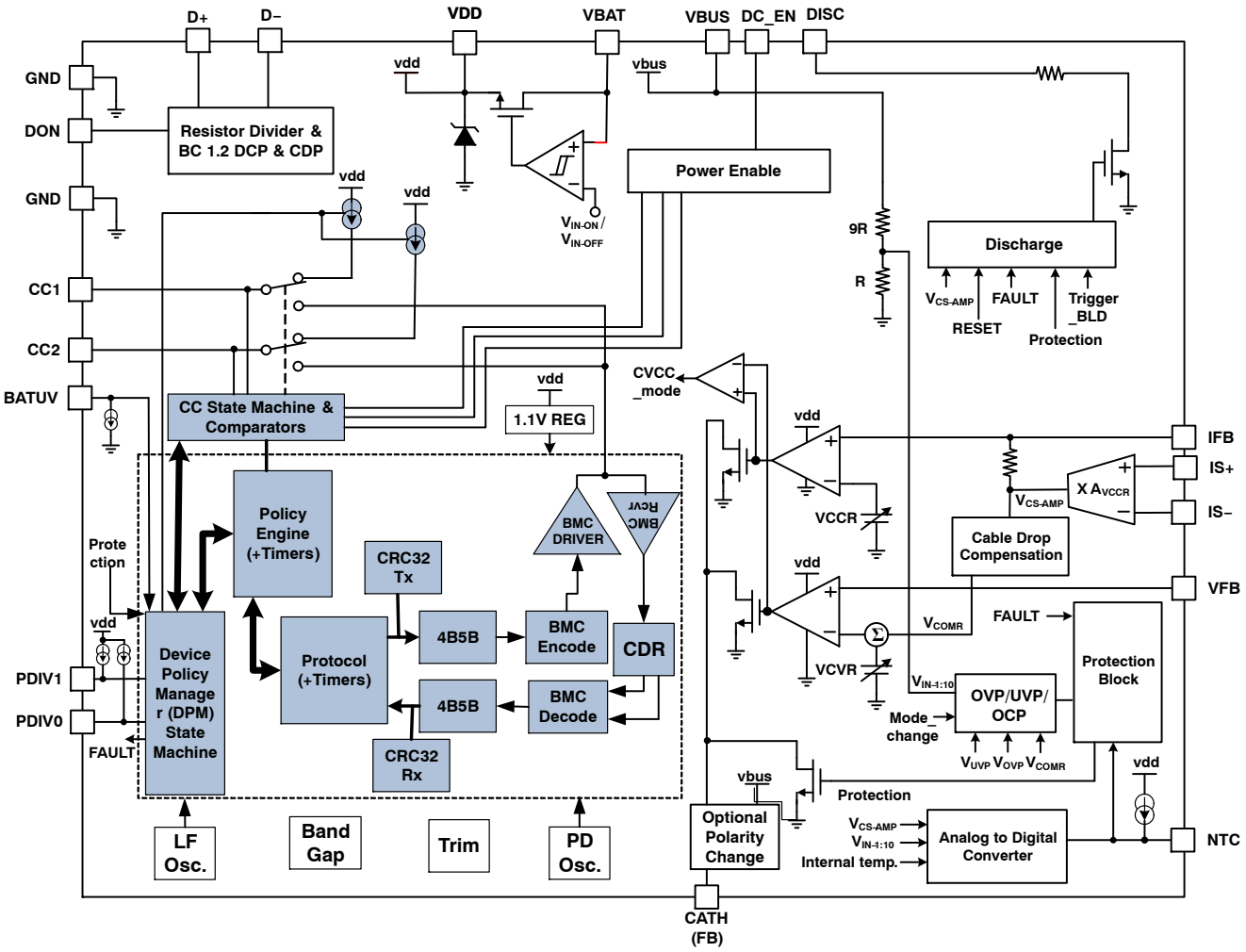


Figure 2. Simplified Block Diagram

Pin Connections

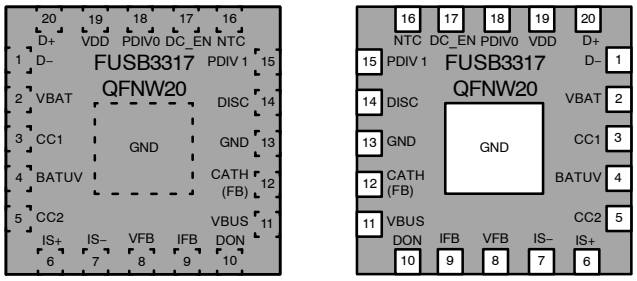


Figure 3. Pinout Diagrams

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O Type	Description
11	VBUS	Input	Output VBUS voltage to the Type C connector (Input voltage to the FUSB3317 to check for OVP and UVP)
2	VBAT	Supply	Input power for the FUSB3317 directly from a battery for automotive applications or from a DC−DC supply for industrial
19	VDD	Output	Supply voltage generated internally from VBAT (output from FUSB3317). This pin is connected to a 1 μF external capacitor.
13	GND	Ground	Connect to board ground but not connector ground
12	CATH(FB)	Open Drain Output	Feedback to control the power supply. Typically connected to the error amplifier output of a DC−DC regulator (often called the compensation pin). For a fuse option, connected to the feedback pin at the resistor divider (FB) of the DC/DC.
8	VFB	Input	Output Voltage Sensing Signal. This pin is used for CV regulation, and it is tied to the internal CV loop amplifier non−inverting input terminal. It is tied to the output voltage resistor divider
9	IFB	Input	Constant Current Amplifying Signal. The voltage level at this pin is the amplified current sense signal.
6	IS+	Input	Current sensing amplifier positive terminal. Connect this pin directly to the positive end of the current sense resistor with a short PCB trace. This is usually the connector ground terminal.
7	IS−	Input	Current sensing amplifier negative terminal. Connect this pin directly to the negative end of the current sense resistor with a short PCB trace. This is usually the board ground.
17	DC_EN	Output	Active High output turns on the DC−DC controller when a Type C Sink is detected.
14	DISC	Open Drain Output	Discharge pin. This pin is tied to VBUS with a discharge resistor in the path to discharge VBUS at the connector.
3	CC1	I/O	Configuration Channel 1. This pin is used to detect USB Type−C devices and communicate over USB PD.
5	CC2	I/O	Configuration Channel 2. This pin is used to detect USB Type−C devices and communicate over USB PD.
20	D+	D+: I/O	D+: Connected to D+
1	D−	D−: I/O	D−: Connected to D−
15	PDIV1	Input	Programmable pin to select different USB Power Delivery Power (PDP) value dynamically
18	PDIV0	Input	Programmable pin to select different USB Power Delivery Power (PDP) value dynamically
16	NTC	I/O	Pin connected to external NTC resistor to sense PCB or connector temperature
10	DON	Output	For USB 2.0 data, this pin is tied to the Switch Control of the USB 2.0 data switch to turn the switch on (5 V HIGH = Switch ON)
4	BATUV	Input	Determines a threshold at which FUSB3317 will scale down the advertised power since the battery voltage is too low

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VBAT Battery Pin Voltage (Note 1)	$V_{VBATMAX}$	−0.3 to 54	V
Connector Pins Voltage: VBUS, DISC, CATH, CC1, CC2, D+ and D−	$V_{HIGHMAX}$	−0.3 to 27 V	V
Low Voltage Pins: DC_EN, DON, IS−, VFB, IFG, BATUV, NTC, PDIV1 and PDIV0	V_{LOWMAX}	−0.3 to 6 V	V
Supply Output Range on Pin VDD	V_{VDDMAX}	−0.3 to 6 V	V
Current Sense Input on Pin IS+	V_{IS+MAX}	IS− + 0.1	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	750	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFNW20, 4x4 mm^2 (Note 1) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Case (Note 4)	 $R_{\theta JA}$ $R_{\theta JC}$	 36.1 2.3	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input VBAT Voltage	V_{VBAT}	4.5	45	V
I/O VBUS Voltage	V_{VBUS}	3.13	22.05	V
Output VDD Supply Voltage	V_{VDD}	4.75	5.5	V
I/O CC1 and CC2 Voltage	V_{CC1CC2}	0	5.5	V
I/O D+ and D− Voltage	V_{D+D-}	0	3.6	V
I/O PDIV0 and PDIV1 Voltage	$V_{PDIV0-1}$	0	5.5	V
I/O NTC Voltage	V_{NTC}	0	5.5	V
Output DON and DC_EN Voltage	V_{DONEN}	0	5.5	V
Output Current as sensed by IS+ to IS− with 5 mΩ resistor	I_{out}	0	5	A
Ambient Temperature	T_A	−40	85 (Commercial) 105 (Automotive)	°C
Junction Temperature	T_J	−40	135	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

For typical values, V_{VVBAT} = 12 V and T_A = 25°C. For min/max values, V_{VVBAT} = 5.5 V to 36 V and T_J = −40°C to 125°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VBAT Input Supply Section						
Turn−On Threshold Voltage	V_{VBAT} rising	V_{BAT-ON}	3.7	4.2	4.7	V
Turn−Off Threshold Voltage	V_{VBAT} falling	$V_{BAT-OFF}$	3.4	3.9	4.4	V
Operating Supply Current at 5.5 V	V_{VBAT} = 5.5 V, VCS=15 mV, Rcs = 5 mΩ	$I_{BAT-OP-5.5V}$		2.5		mA
Operating Supply Current at 36 V	V_{VBAT} = 36 V, VCS=15 mV, Rcs = 5 mΩ	$I_{BAT-OP-36V}$		4		mA
Standby Power Operating Supply Current	V_{VBAT} = 12 V, VIS+ = VIS− = 0 V	I_Q		100		μA
VBAT Under Voltage Protection (UVP) Section						
VBAT Under Voltage Threshold	BATUV pin is floating	$V_{BAT-UVP}$	3.8		5.9	V
BATUV Pin Voltage Threshold to Trigger Battery UVP	BATUV pin with resistor divider to VBAT pin	V_{BAT-TH}	0.56	0.6	0.64	V
UVP Detection Debounce Timing (Note 8)	V_{VBAT} falling	$t_{VBATUV-DEB}$	0		2	ms
VDD Output Supply Section						
VDD Output Voltage	V_{VBAT} range 5.5 to 36 V	V_{DD}	4.5	5.0	5.5	V
VDD Source Current	V_{VBAT} = 12 V, current when V_{DD} = 4.5 V	I_{DD}	10			mA
VBUS Under Voltage Protection (UVP) Section						
Ratio V_{VBUS} Under−Voltage−Protection (UVP) to V_{CC}	V_{VBUS} falling	$V_{BUS-UVP-65}$	61	65	69	%
Turn−Off Threshold Voltage	V_{VBUS} falling in a PPS contract	$V_{BUS-UVP-PPS}$	2.805	2.97	3.135	V
UVP Debounce Time	V_{VBUS} falling	$t_{D-VBUS-UVP}$	45	60	75	ms
UVP Blanking Time	Whenever a voltage change occurs from lower V_{VBUS} to a higher V_{VBUS}	$t_{BNK-UVP}$	160	200	240	ms
VBUS Over Voltage Protection (OVP) Section						
VBUS Over Voltage Protection Threshold	VBUS rising	$V_{BUS-OVP-120}$	116	120	127	%
VBUS OVP Debounce Time	VBUS rising	$t_{D-VBUS-OVP}$	35	75	115	μs
VBUS OVP Blanking Time (Note 5)	During VBUS voltage transition of voltage step ≤ 0.5V, final V_{VBUS} ≥ 13V	$t_{BNK-OVP-11}$	5.5	7	8.5	ms
VBUS OVP Blanking Time (Note 5)	During VBUS voltage transition of voltage step ≤ 0.5V, final V_{VBUS} < 13V	$t_{BNK-OVP-10}$	51	55	60	ms
VBUS OVP Blanking Time (Note 5)	During VBUS voltage transition of voltage step > 0.5V, final V_{VBUS} ≥ 13V	$t_{BNK-OVP-01}$	16.5	19	21.5	ms
VBUS OVP Blanking Time (Note 5)	During VBUS voltage transition of voltage step > 0.5V, final V_{VBUS} < 13V	$t_{BNK-OVP-00}$	205	221	236	ms
Constant Current Limit (CC or CL) Sensing Section						
Current−Sense Amplifier Gain	Current sense resistor, Rcs = 5 mΩ	A_{V-CCR}		40		V/V
Current range when controlling current limit at I_{OUT} = 1.00 A	PPS constant current limit mode at 1 A	$I_{CS-1.00A}$	0.85	1.00	1.15	A
Current range when controlling current limit at I_{OUT} = 2.00 A	PPS constant current limit mode at 2 A	$I_{CS-2.00A}$	1.85	2.00	2.15	A
Current range when controlling current limit at I_{OUT} = 3.00 A	PPS constant current limit mode at 3 A	$I_{CS-3.00A}$	2.85	3.00	3.15	A
Current range when controlling current limit at I_{OUT} = 4.00 A	PPS constant current limit mode at 4 A	$I_{CS-4.00A}$	3.80	4.00	4.20	A
Current range when controlling current limit at I_{OUT} = 5.00 A	PPS constant current limit mode at 5 A	$I_{CS-5.00A}$	4.75	5.00	5.25	A

ELECTRICAL CHARACTERISTICS (continued)
For typical values, V_{VVBAT} = 12 V and T_A = 25°C. For min/max values, V_{VVBAT} = 5.5 V to 36 V and T_J = −40°C to 125°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Over Current Protection (OCP) Sensing Section						
Over Current Protection (OCP) threshold percentage of maximum current	PD request for constant voltage mode with VBUS at 5.2 V and 3 A maximum current	$I_{OCP-PER}$	109	120	124	%
OCP debounce time	Constant current exceeding $I_{OCP-PER}$	$t_{OCP-DEB}$	50	60	70	ms
Current threshold on sensing resistor for enabling discharge on DISC pin during a voltage transition	VBUS is decreasing	$I_{CS-DSCG}$		430		mA
Debounce time for enabling discharge on DISC pin during a voltage transition	VBUS is decreasing	$t_{CS-DSCG}$		0.6	1.0	ms
Constant Voltage Sensing Section						
VFB Reference Voltage at 3.3 V	VBUS = 3.3 V, current sense resistor voltage, Vcs = 0 V	$V_{CVR-3.3V}$	0.32	0.33	0.34	V
VFB Reference Voltage at 5.2 V nominal output voltage	VBUS = 5.2 V, current sense resistor voltage, Vcs = 0 V	V_{CVR-5V}	0.504	0.520	0.536	V
VFB Reference Voltage at 9 V nominal output voltage	VBUS = 9 V, current sense resistor voltage, Vcs = 0 V	V_{CVR-9V}	0.873	0.900	0.927	V
VFB Reference Voltage at 15 V nominal output voltage	VBUS = 15 V, current sense resistor voltage, Vcs = 0 V	$V_{CVR-15V}$	1.455	1.500	1.545	V
VFB Reference Voltage at 20 V nominal output voltage	VBUS = 20 V, current sense resistor voltage, Vcs = 0 V	$V_{CVR-20V}$	1.940	2.000	2.060	V
Feedback Section						
CATH(FB) pin sink/source current (Note 5)	CATH(FB) as a sink (Note 6)	$I_{CATH-SNK}$	2			mA
CATH(FB) pin sink/source current (Note 5)	CATH(FB) as a source (Note 6)	I_{FB-SRC}			−2	mA
Discharge Section						
VBUS to GND Leakage Resistance	DC_EN = 0 V, VBUS not sourced	$R_{DISC-VBUS}$	72.4	155		kΩ
VBUS Pin Sink Current	VBUS = 20 V and being discharged	$I_{DISC-SNK}$	250			mA
Discharge Time	During VBUS voltage transition of voltage step ≤ 0.5 V, final V_{VBUS} > 13 V	$t_{DISC-11}$	5.5	7	8.5	ms
Discharge Time	During VBUS voltage transition of voltage step ≤ 0.5 V, final V_{VBUS} < 13 V	$t_{DISC-10}$	51	55	60	ms
Discharge Time	During VBUS voltage transition of voltage step > 0.5 V, final V_{VBUS} > 13 V	$t_{DISC-01}$	16.5	19	21.5	ms
Discharge Time	During VBUS voltage transition of voltage step > 0.5 V, final V_{VBUS} < 13 V	$t_{DISC-00}$	205.5	221	236.5	ms
Over Temperature Protection (OTP) Section						
Current Source on NTC Pin	Resistance to ground on NTC = 3.293 kΩ	I_{NTC}	55	60	65	μA
Debounce Time for External Over Temperature Protection (E_OTP)	Over temperature event	$t_{NTC-DEB}$		90		ms
Over Temperature Warning Threshold on NTC pin at 100°C (Note 8)	Resistance to ground on NTC = 4.247 kΩ	$V_{NTC-WARN}$	0.234	0.256	0.276	V
Over Temperature Protection Threshold on NTC pin at 100°C (Note 8)	Resistance to ground on NTC = 3.293 kΩ	$V_{NTC-OTP}$	0.181	0.198	0.214	V
Internal Over Temperature Protection (I_OTP) Threshold (Note 8)		T_{I_OTP}		135		°C

ELECTRICAL CHARACTERISTICS (continued)
For typical values, V_{VVBAT} = 12 V and T_A = 25°C. For min/max values, V_{VVBAT} = 5.5 V to 36 V and T_J = −40°C to 125°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Protection Recovery Section						
Duration after Fault Removed before Normal Operation Resumes (Note 5)	Any fault applied and then removed and not in debug accessory operation	$t_{2S-AR-NM}$	1.8	2.0	2.2	s
Duration after Fault Removed before Normal Operation Resumes (Note 5)	Any fault applied and then removed and debug accessory has been detected	$t_{2S-AR-DM}$		100		ms
OCP debounce time used for both detecting an OCP or Current limit condition		$t_{OCP\_Debounce}$	50	60	70	ms
Inputs and Outputs Section						
Input LOW Voltage for PDIV1 and PDIV0	PDIVx voltage swept from 0 V to 5.5 V	$V_{IL-PDIVx}$			0.4	V
Input HIGH Voltage for PDIV1 and PDIV0	PDIVx voltage swept from 0 V to 5.5 V	$V_{IH-PDIVx}$	V_{VDD} − 0.4			V
Output LOW Voltage for DON and DC_EN	Sink current = 1 mA	V_{OH}			0.4	V
Output HIGH Voltage for DON and DC_EN	Source current = −1 mA	V_{OH}	2.0			V
Type C USB Section						
CC1 or CC2 Pull−Up Current for 3A	V_{VBAT} = 12 V, CC1 and CC2 floating	I_{CCx-3A}	304	330	356	μA
Open Circuit Impedance on CC1 or CC2	V_{VBAT} = 12 V, disabled state	$Z_{OPEN-CCx}$	126			kΩ
Ra Detection Voltage Threshold	CCx swept from 5.5 V to 0 V, I_{CCx-3A} applied	$V_{Ra-CCx-3A}$	0.75	0.8	0.85	V
Rd Disconnect Detection Voltage Threshold	CCx swept from 5.5 V to 0 V, I_{CCx-3A} applied	$V_{Rd-CCx-3A}$	2.45	2.60	2.75	V
Debounce Time before SRC Detection	Rd connected to CC1 or CC2	$t_{CCx-DEB}$	100	150	200	ms
V_{CONN} Voltage Range	When eMarker being discovered	V_{VCONN}	3.0		5.5	V
V_{CONN} Current Supplied	When eMarker being discovered	I_{VCONN}	34			mA
V_{CONN} Over Current Protection Threshold	When eMarker being discovered	$I_{VCONN-OCP}$	50			mA
CC1 or CC2 Over Voltage Protection		V_{CC-OVP}	5.5	5.75	6.0	V
CC1 or CC2 OVP Debounce Time		$t_{CCOVP-DEB}$			100	μs
D+ or D− Over Voltage Protection		$V_{DPDM-OVP}$	4.1	4.35	4.6	V
D+ or D− OVP Debounce Time		$T_{DPDM-OVP-DEB}$			4.5	ms
USB Power Delivery BMC Section						
BMC Period		t_{UI}	3.03		3.7	μs
BMC Transmitter Rise Time		$t_{RISE-BMC}$	300			ns
BMC Transmitter Fall Time		$t_{FALL-BMC}$	300			ns
BMC Transmitter Driver Impedance		z_{DRIVER}	33		75	Ω
BMC Receiver Bandwidth Limiting Filter		$t_{RX-FILTER}$	100			ns
BMC Receiver Capacitance (Note 5)	BMC driver is not turned on	$c_{RECEIVER}$		15		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C
6. Refer to the APPLICATION INFORMATION section.
7. Values based on design and/or characterization.
8. Guaranteed by design/characterization.

APPLICATIONS INFORMATION

FUSB3317 has the entire Power Delivery (PD) communication stack within hardware including the optional Programmable Power Supply (PPS). No external processor is needed. This enables turnkey solutions for PD with PPS and makes this solution tamper proof unlike other firmware−based solutions.

VBAT Supply Input

Connect the automotive battery supply directly to the VBAT pin of the FUSB3317. The battery voltage can vary from 5.5 V to 36 V in normal operation but can be up to 45 V for short periods of time when an automotive load dump event occurs. Similarly, the battery voltage could dip to 4.5 V momentarily. If there is significant dropout of VBAT for tens of microseconds or milliseconds, an input holdup capacitor is needed to stabilize VBAT to be within the above voltage range.

Low Standby Current

With the FUSB3317 connected directly to the battery, there is no need to turn on the DC/DC unless there is something attached to the USB−C port. The FUSB3317 will consume very low current (I_Q) while looking for a Sink attach allowing for a very low system standby current.

Local Power Generated

FUSB3317 generates its own power from VBAT via an integrated LDO. The total current generated can be consumed by the FUSB3317 and by external low−power electronics as long as the combined current is less than I_{DD}. The recommended external decoupling capacitor on V_{DD} is 2.2 μF or greater. The value of V_{DD} is typically 5.2 V.

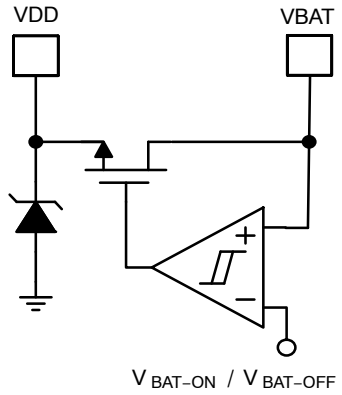


Figure 4. VDD LDO Supply Generation

Type C Attach

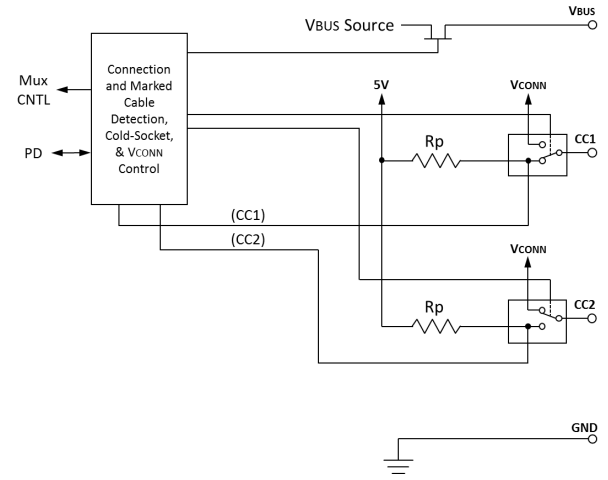


Figure 5. Type C Source

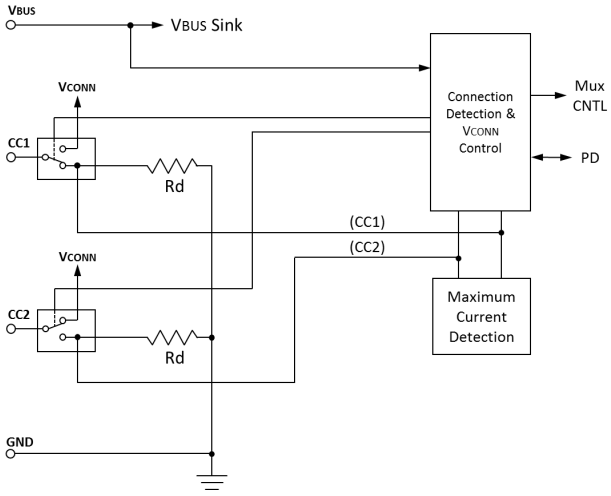


Figure 6. Type C Sink

The FUSB3317 implements the Rp pull up resistors in Figure 5 as current sources ($I_{CCx−3A}$) that advertise 3A default current capability. When the Sink's CC1 or CC2 pins as shown in Figure 6 with Rd as 5.1 kΩ resistor connect with either with CC1 or CC2 of the FUSB3317 in a flipped or straight connection, an attach occurs when the voltage on the CC1 or CC2 pin (only one CCx connects through the cable) is in the $V_{Rd−CCx−3A}$ range. Once this attach is detected, FUSB3317 enables a DC/DC controller via DC_EN pin to source VBUS provided the connector VBUS pin is initially discharged to ground (VBUS not source if VBUS already present).

USB Power Delivery Support

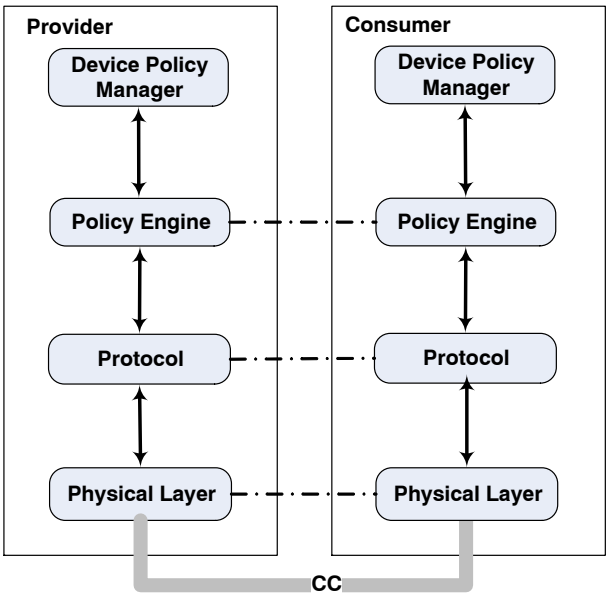


Figure 7. USB−PD Communication Stack

USB Power Delivery (PD) provides a way for a Source and Sink to negotiate output power settings, allowing for increased power delivery up to 100 W for Standard Power Range (SPR). USB PD uses the CC signal that is passed through the cable to provide the link between the Source and the Sink to send messages and commands. The communications stack consists of Physical, Protocol, Policy Engine and Device Policy Manager layers as shown in Figure 7 where each layer in the FUSB3317 talks to its corresponding layer in the Sink device.

The Physical (PHY) Layer handles both the transmission and reception of the bits on the CC signal. All data is first encoded using a 4b5b line code and then transmitted across the CC signal using Biphase Mark Coding (BMC). A 32 − bit CRC is also used to protect the data integrity of the data payload.

The Protocol Layer defines how USB PD messages are constructed and used between a Source device and a Sink device. All USB PD messages must follow a strict packet definition and may also include timing requirements based on the type of message. The Protocol Layer is responsible for verifying the timing parameters and handling any communication errors as they arise.

The Policy Engine (PE) is responsible for executing the device Local Policy to control its power delivery behavior. The Policy Engine defines a set of message sequences that must be followed for proper operation. All power negotiations are handled by the Policy Engine.

The Device Policy Manager (DPM) is responsible for overseeing the power supply and managing changes to the Local Policy, including handling of alert and fault conditions. It is also responsible for managing VCONN and the Discover Identity messaging to determine the full capabilities of the cabling.

FUSB3317 consists of all four PHY, Protocol, PE and DPM layers to fully implement a compliant PD Source fully in hardware.

USB PD Power Advertisement

The USB PD specification defines Power Data Objects (PDO) and Augmented Power Data Objects (APDO) as a way for the Source device to advertise it's power capabilities. PDO's describe well − regulated fixed voltage supplies while APDO Programmable Power Supply (PPS) describe a power supply whose output voltage can be adjusted over the advertised voltage range. A Source can advertise a combination of PDOs and APDOs, up to a maximum of 7 total Data Objects for SPR. In order to provide a consistent experience across the Source devices with the same PD Power (PDP) rating, a set of power rules are contained within the PD specification. The power rules provide a set of minimum requirements (PDOs and APDOs) that must be met for a Source device based on the advertised PDP.

The FUSB3317 can be configured to meet a variety of different PDP power advertisements, depending on the application requirements. The default power for the FUSB3317 is the standard 60 W option as shown in Table 1.

Table 1. FUSB3317 DEFAULT PDOs AND APDOs

[A]PDO Power Data Object	Output Voltage	Max Current w/3 A Cable	Current Mode
PDO1	5 V	3.6 A	OCP
PDO2	9 V	3.6 A	OCP
PDO3	15 V	3.6 A	OCP
PDO4	20 V	3.6 A	OCP
APDO1	3.3 V ~ 21 V	3 A	CL or CC

Constant Voltage Control

In order to regulate adaptive output voltages, the constant voltage control (CV) is implemented. The output voltage is sensed through an external resistor divider. The sensed output voltage is connected to the VFB pin, and it is input the non − inverting input terminal of the internal operational amplifier. The inverting input terminal is connected to the internal voltage reference (V_{CVR}) which can be adjusted according to the requested output voltage. The amplifier and an internal switch operate as a shunt regulator, and the output of the shunt regulator is connected to the CATH pin. To compensate output voltage regulation, typically, two capacitors and one resistor are connected between CATH and VFB pins as Figure 8. The output voltage can be derived as calculated by the Equation 1, and the ratio of the resistor divider is 10. The reference (VCVR) for the output voltage is generated by a 10 − bit DAC. The minimum resolution is 20 mV to meet PD compliance for PPS.

$$V_{VBUS} = V_{CVR}\left(\frac{R_{F1} + R_{F2}}{R_{F2}}\right) \quad \text{(eq. 1)}$$

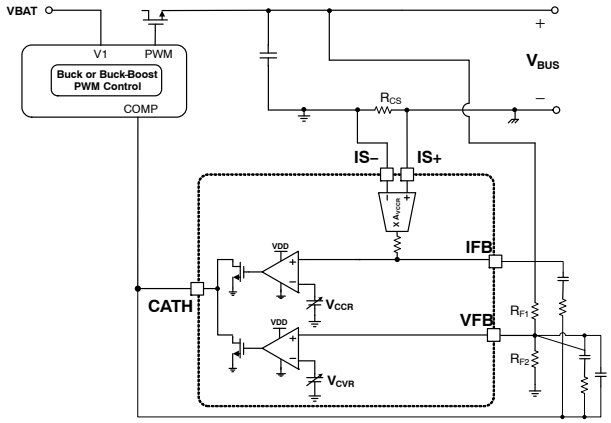


Figure 8. Voltage and Current Sensing Circuits

Constant Current Control

Constant Current Limit (CL or CC) or control is enabled during USB PD explicit contracts with a PPS APDO. When CL (or CC) mode is enabled, the supply will decrease the output voltage as the load increases in order to maintain a fixed output current. Output current is sensed via a current − sense resistor R_{CS}, which is connected between the IS+ and IS− pins. The sensed signal is internally amplified, and this amplified voltage is connected to the non − inverting input of the internal operational amplifier. Similar to the constant voltage amplifier circuit, it also plays a role as a shunt regulator to regulate the constant output current. In order to compensate output current regulation, one capacitor and one resistor are connected between the IFB and CATH pins as shown in Figure 8. The constant output current can be calculated using Equation 2. 5 mΩ is typically used for the sense resistor.

$$I_{CS} = \frac{1}{40}\left(\frac{V_{CCR}}{R_{CS}}\right) \quad \text{(eq. 2)}$$

Since the voltage across the IS+ and IS− pins is small, the sensing resistor should be positioned as close as possible to the pins. An RC filter can be added to the pins to reduce the noise seen on the circuit.

Output Over Current Protection

Over Current Protection (OCP) is enabled during USB PD explicit contracts with PDOs (i.e. not PPS APDOs). When OCP mode is enabled, the supply will regulate the output voltage until the load current exceeds the OCP threshold, at which point it will cause a fault condition and disable the output voltage and disconnects from the attached Sink. Similar to Constant Current Control, the FUSB3317 detects the output current via the current sense resistor RCS, with the difference being the output of the CC amplifier disconnected from the CATH signal. When the load current exceeds the OCP threshold for longer than tOCP−DEB, OCP is triggered and the FUSB3317 enters Auto Restart Mode after OCP is not detected.

Discharge Functionality

Discharge circuits are implemented on the DISC pin to discharge the output capacitors quickly during voltage and/or current transitions and to fully discharge VBUS when required. The discharge circuits in the FUSB3317 are sized to meet the timing requirements in the USB PD specification. Since the output load can discharge the load sufficiently during heavy loads, the discharge circuits are only enabled during light load conditions (ICS< lCS−DSCG). The operation of the discharge circuits is shown in Table 2 and Table 3.

Table 2. DISCHARGE DURING VOLTAGE TRANSITIONS

Step Size	New VBUS	tBDISC−xx (typ)	DC_EN
≤ 0.5 V	>13 V	7 ms	Enabled
	<13 V	19 ms	Enabled
>0.5 V	>13 V	55 ms	Enabled
	<13 V	221 ms	Enabled

Table 3. DISCHARGE UPON DETACH, PROTECTION MODE OPERATION OR HARD RESET

Initial VBUS	Final VBUS	tBDISC−xx (typ)	DC_EN
3.3 V ~ 21 V	vSafe0V (<0.8 V)	221 ms	Enabled

Protection Mode and Auto Restart Operation

The FUSB3317 provides Output Over Voltage Protection (OVP), Under Voltage Protection (UVP), Output Over Current Protection (OCP), External Over Temperature Protection via NTC (E_OTP), Internal Over Temperature Protection (I_OTP), D+/D− line Over Voltage Protection (D_OVP) and CC line Over Voltage Protection (CC_OVP). When a protection mode is triggered, the DC/DC is disabled and the discharge circuits are enabled to protect the Sink device. During this time, the CC pull−up currents (ICCx−3A) are disabled to indicate to the Sink device that the Source is not ready to provide power. The functionality described is shown in Figure 9. Once the fault conditions are removed, the FUSB3317 will re−enable the DISC discharge circuit and begin the auto − restart timer (t2S−AR−NM). After the auto − restart timer expires, the CC pull − up currents will be enabled to allow a Sink device to attach.

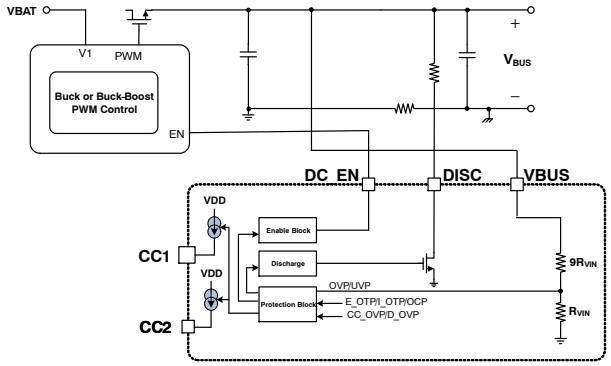


Figure 9. Protection Block Diagram

DC_EN

DC_EN pin is to disable/enable the external VBUS supply IC like DC−DC converter. So, DC_EN connects to Enable pin of DC−DC converter. To minimize the current consumption of DC−DC converter while Sink is not plugged in, FUSB3317 turns off the DC−DC until sink device attaches. Once Sink attaches, FUSB3317 detects the CC attach and enables DC_EN to High after 100msec of CC debounce to supply VBUS. Also the CATH pin controls the VBUS to 5 V default along with the DC_EN The initial VBUS will be 5 Volt by default feedback and the voltage can be changed following PD contract over CATH. DC_EN is controlled to Low with sink detach or device reset by POR or protection mode from OVP/OCP/OTP.

DON and USB2.0 Data Lines

The USB 2.0 Data Lines, D+ and D−, can be externally connected together via a 100 ohms resistor to provide the maximum power, a legacy USB device can take, which is 1.5 A per USB Battery Charging v1.2 (BC1.2) specification. This will usually be the case when a USB−C to micro−B cable is plugged into this design where this adapter cable has the required Sink Rd resistors within it to allow the FUSB3317 to recognize a Type C attach and to source 5 V on VBUS. The Sink will go through BC1.2 steps of primary and secondary detection to detect a Dedicated Charging Port (DCP) via this resistor connection of D+ and D− and takes 1.5 A maximum from VBUS.

Internally, FUSB3317 presents BC1.2 Charging Downstream Port(CDP) mode in default to provide the 1.5 A of power as well as to make USB signal path connection between USB PHY, Head unit in automotive application and sink device. Since USB data, D+, D−, path have to connect from Sink to FUSB3317 as well as head unit, there should be 2:1 switch mux externally. DON pin of FUSB3317 can control the external switch enable or switch direction control. Below diagram is the example of using external switch, NIV1241, which has signal switch and TVS diodes on D+ and D− for ESD protection.

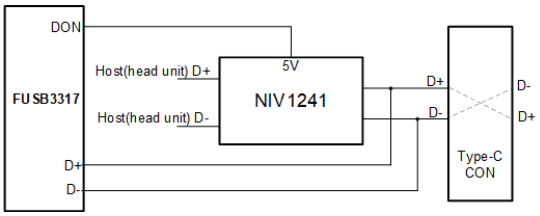


Figure 10. DON Pin Connection to NIV1241

With sink attach, the FUSB3317 controls the DON pin High to close the USB D+/D− signals between head unit and the attached sink. DON pin is controlled to High about 900 ms after CC debounce and stayed high until sink device is plugged out. DON pin controls to Low with sink detach or device reset by POR or protection mode from OVP/OCP/OTP.

BATUV

BATUV pin monitors VBAT, battery voltage, to know if the voltage is low enough to send a new PD message to scale down the negotiated source power data object. The pin can be left float or either resistor divide input of VBAT. When the BATUV is float, if VBAT is below V_{BAT_UVP}, max 5.9 V, or when the BATUV is resistor divide of VBAT and then if the BATUV drops below, V_{BAT_TH}, 0.6 Volt, the new PD message will be sent to sink to renegotiate. In both cases, the 2 ms debounce time, t_{VBATUV_DEB}, is applied before sending scale down message. The scaled down PDP(Power Delivery Power) by VBAT UVP will be 75% of the max PDP. For example, at 60 W PDP default, it will change to 45 W by VBAT UVP. Once VBAT UVP is recovered, it will come back to 60 W.

NTC

NTC pin is to detect external temperature on the board. NTC will connect to a thermistor which can be placed in the hottest place on the PCB, it could be next to NFET or close to the USB−C connector. Once NTC temperature rises to warning range which is 90°C, the scale down PDP will be sent to sink so that the sink will pull less current/power. The scale is the same as VBAT UVP, 75%. If the NTC detects above shut down temperature, 100°C, FUSB3317 enters fault protection mode and VBUS FET will be shut off and Sink will be disconnected.

The new PDP table is below in case of either VBAT UVP or NTC. The PDP scaling minimum is 25% of PDP and PDP scaling default is 75%.

VBAT−UVP	NTC Warning	Resultant_PDP
Yes	No	PDP_scaling*Current_PDP
No	Yes	PDP_scaling*Current_PDP
Yes	Yes	PDP_scaling minimum *Current_PDP
No	No	Current_PDP

PDIV0, PDIV1

These pins are prepared in addition to the fuse bits to provide a PDP range of 7.5W to 100W. FUSB3317 changes PDP dynamically once either PDV1 or PDIV0 is changed so the new PD message will be sent by the voltage change of PDIVx. The table below is PDP setting logic by PDIVx.

PDIV1:PDIV0	Current_PDP of FUSB3317
11	100%*max_power_PDP
10	75%*max_power_PDP
01	50%*max_power_PDP
00	25%*max_power_PDP

VDD

VDD is 5 V regulator output, please add 2.2 μF capacitor on the pin. Detail description and block diagram are mentioned above.

Vconn Over current protection (Vconn OCP)

FUSB3317 will turn on VCONN whenever it needs to read the eMarker in the cable only if 5 A capability is supported by trim option. When VCONN is sourced, per USB PD specification only 100 mW maximum (5 V with 20 mA for the FUSB3317) needs to be supplied for a USB 2.0 source application. If the VCONN current exceeds ICONN_OCP (typical 50 mA) for tVCONN_OCP then the FUSB3317 will disable the VCONN supply and abort the eMarker discovery process. The default maximum current of 3 A will be used for all source capabilities for USB PD messages in the latter case and the normal PD messaging will occurs without interruption. No Alert messages will be sent but the PD Status message will have a bit to indicate that the cable limited the FUSB3317 from advertising 5 A source capabilities.

CC1 and CC2 Over Voltage Protection (CC_OVP)

FUSB3317 protects against the CC1 and CC2 connector pins being shorted to VBUS up to 27 V and it has the ability to start protecting the system when the CC voltage is beyond it normal operating range. If either CC1 or CC2 voltage is above, $V_{CC-OVP,}$ OVP threshold for $t_{CC-OVP-DEB}$, then the FUSB3317 protects the system by triggering this fault and executing protection as described in Protection Operation section above.

D+/D− Lines Over Voltage Protection

In order to protect the FUSB3317 when D+ or D− are short−circuited with small impedance to VBUS, OVP is incorporated on D+ and D− pin. If voltage on D+ and/or D− is greater than $V_{DPDM-OVP}$ and the OVP is longer than, $t_{DPDM-OVP-DEV,}$ OVP debounce, D+/D− line Over−Voltage Protection is triggered. D+/D− OVP is always enabled in default. D+ and D− lines have absolute voltage up to 27 V so that any short to VBUS when VBUS is at its OVP limit will not destroy the D+ and D− pins since it takes a finite amount of time after recognizing an OVP on VBUS or D+/D− before the DC/DC controller is shut off and VBUS capacitance is discharged.

DISC

DISC pin connects to VBUS path between NFET source pin and VBUS pin of USB−C connector through about 40 Ω series resistor to discharge VBUS capacitor when VBUS changes from high to low, like 15 V to 5 V. The force discharge can make the VBUS transition fast enough to meet the USB PD spec even with large bulk capacitor. DISC discharge only occurs when VBUS load current is less than about 250 mA, if the load current is larger than that, the DISC discharge doesn't occur. DISC discharge also occurs at fault conditions such as, OVP, UVP, OCP and OTP on VBUS or CCx OVP or DP/DM OVP conditions.

REFERENCES AND DEFINITIONS

Specifications Used in this Datasheet

- Universal Serial Bus Power Delivery specification revision 3.1 version 1.0
- Universal Serial Bus Type C Cable and Connection Specification release 2.0, dated August, 2019
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- Universal Serial Bus Power Delivery specification revision 2.0 version 1.3, dated 12 January, 2017

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops by 10 % with respect to its nominal value.

Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

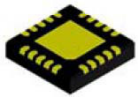
ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Shipping†
FUSB3317V6AMNWTWG	3317V6A	QFNW20 4x4, 0.5P (Pb−Free)	4000 / Tape & Reel
FUSB3317F6AMNWTWG	3317F6A	QFNW20 4x4, 0.5P (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

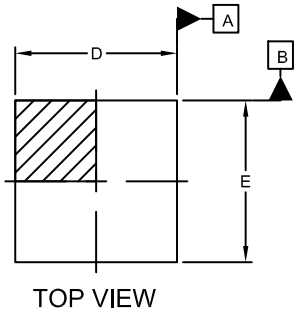
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

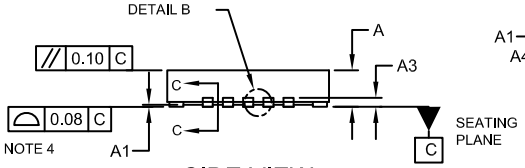


QFNW20 4x4, 0.5P
CASE 484AT
ISSUE O

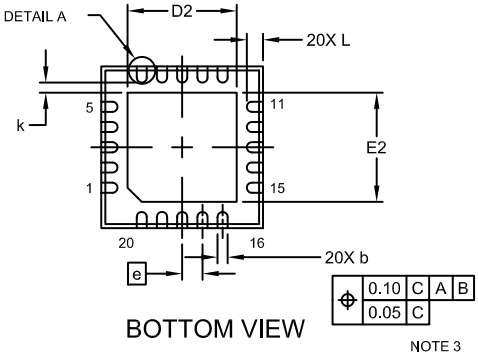
DATE 06 AUG 2019



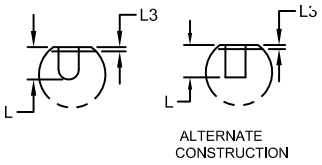
TOP VIEW



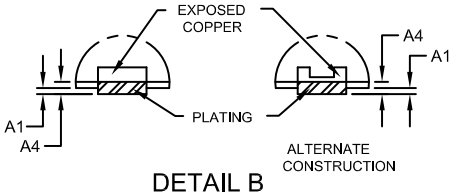
SIDE VIEW



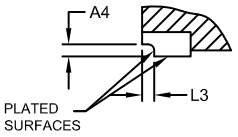
BOTTOM VIEW



DETAIL A



DETAIL B

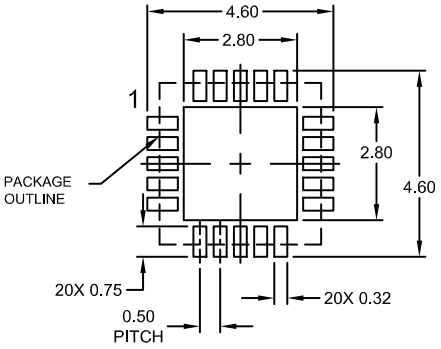


SECTION C-C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2008.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	0.50 BSC		
k	0.20	---	---
L	0.35	0.40	0.45
L3	---	---	0.090



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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